MP 1039026 REV A
MARKING

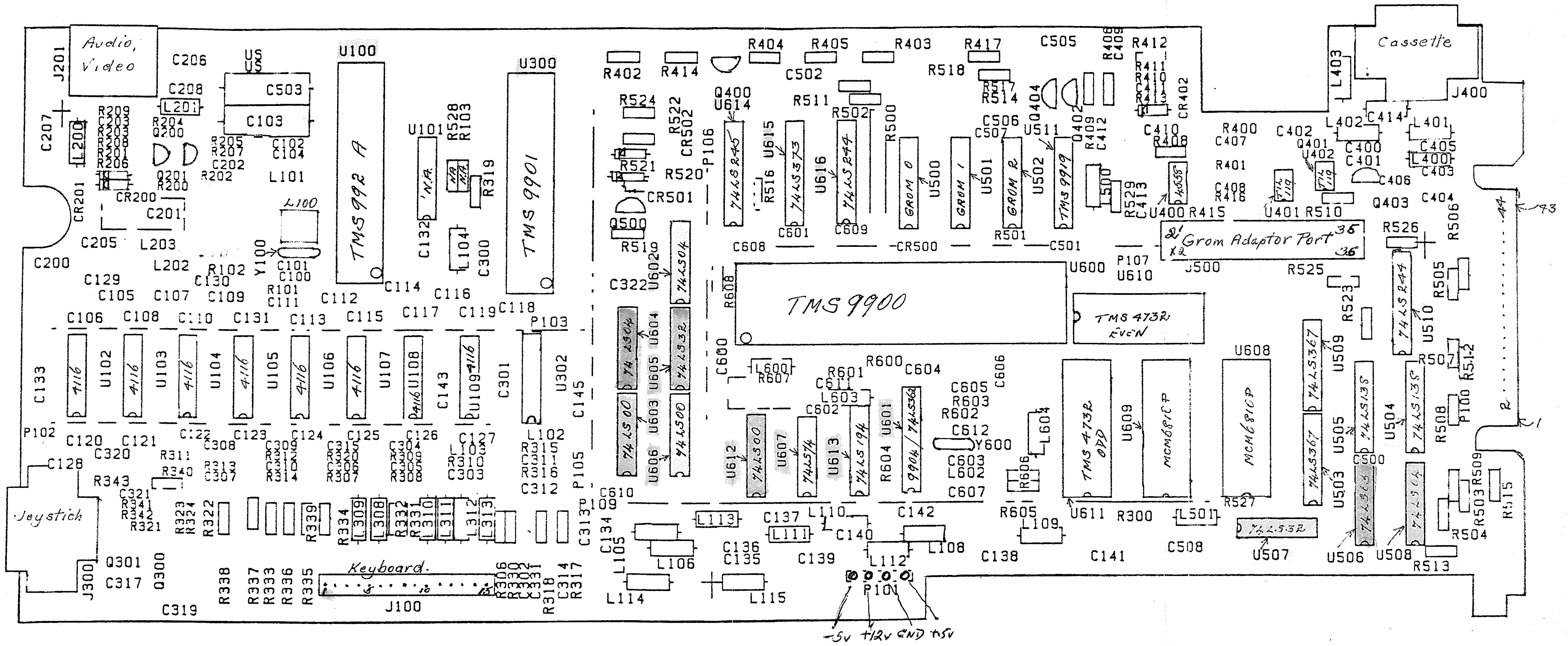


Figure F

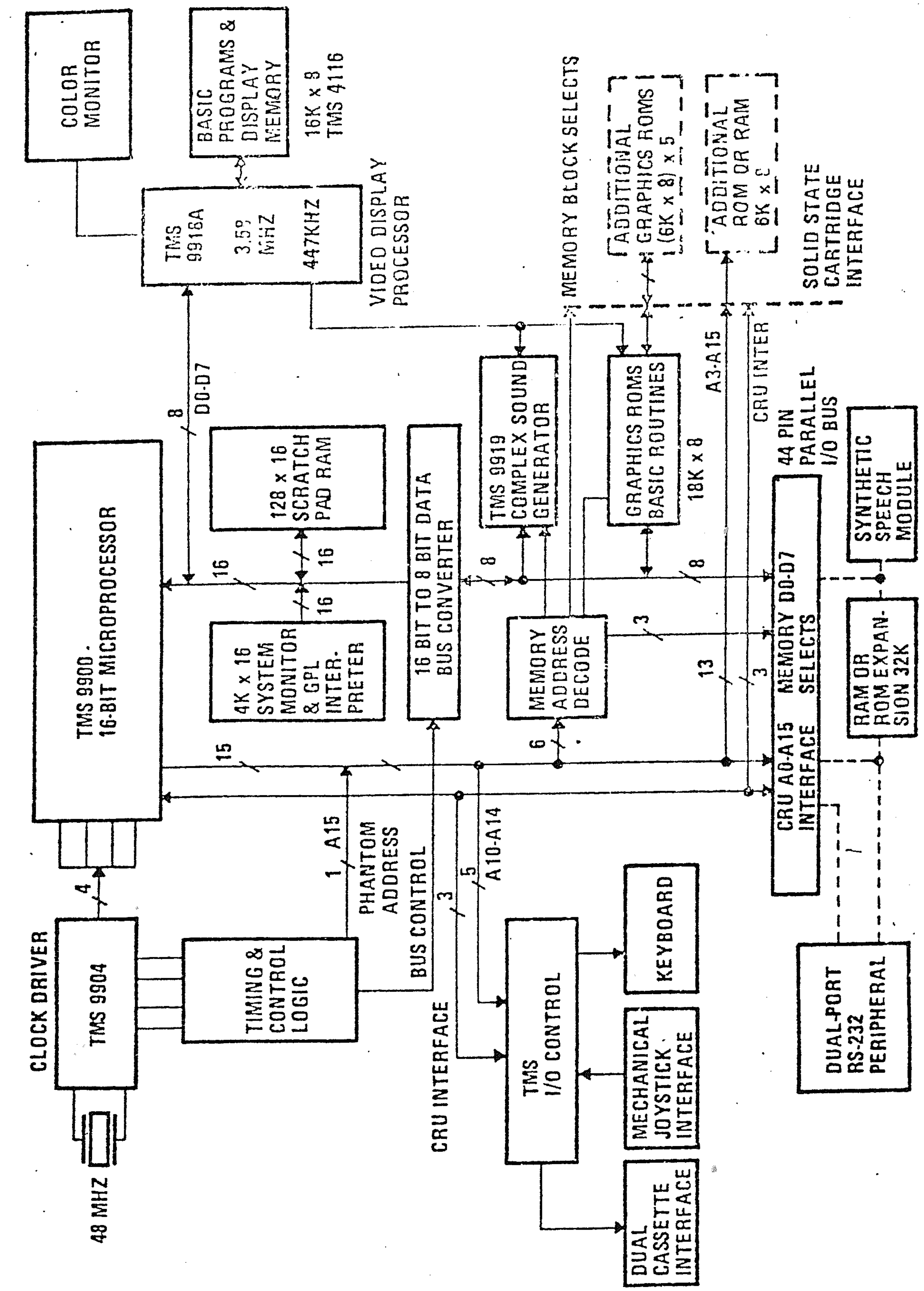


FIGURE A. TI-99/4A SYSTEM BLOCK DIAGRAM

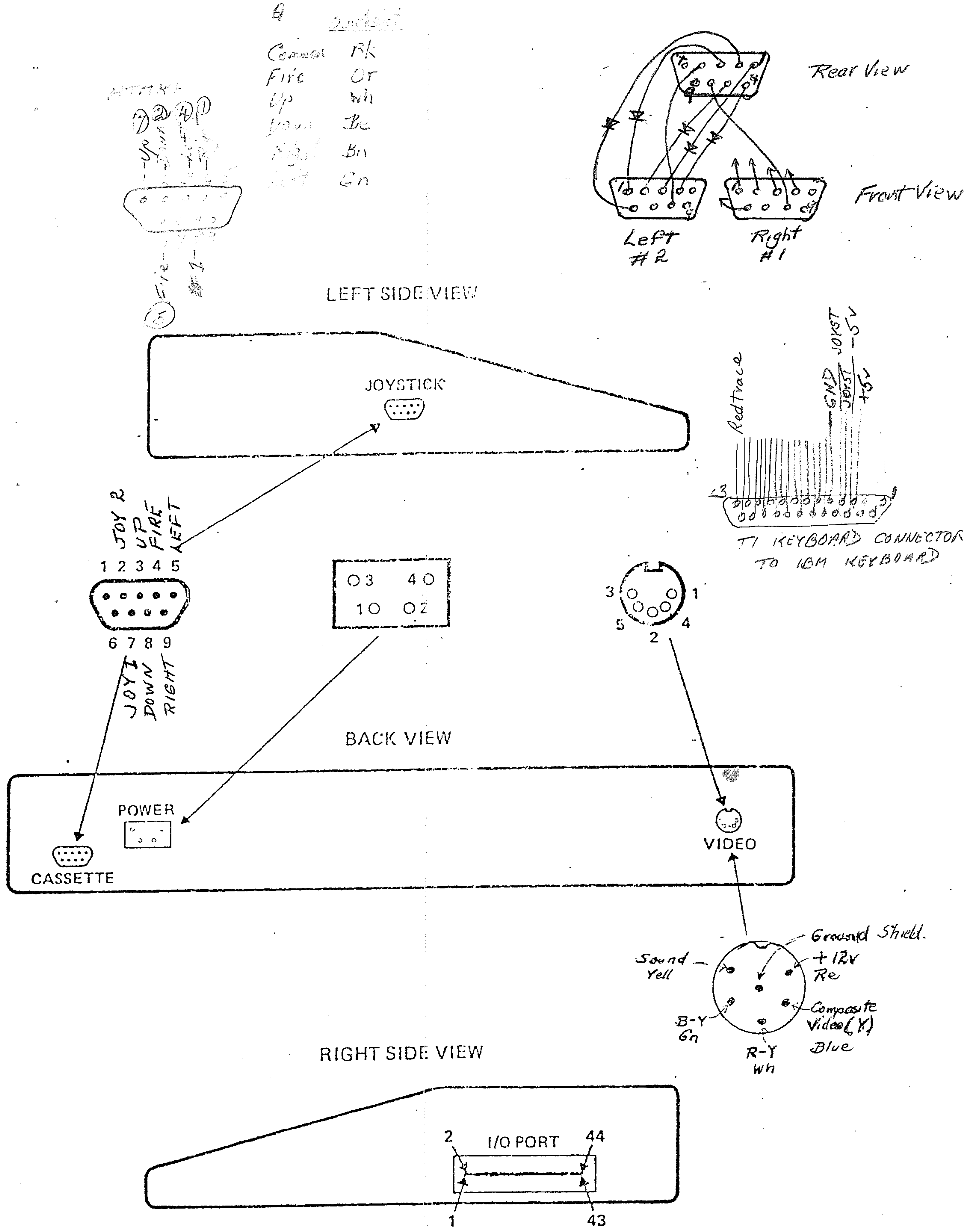
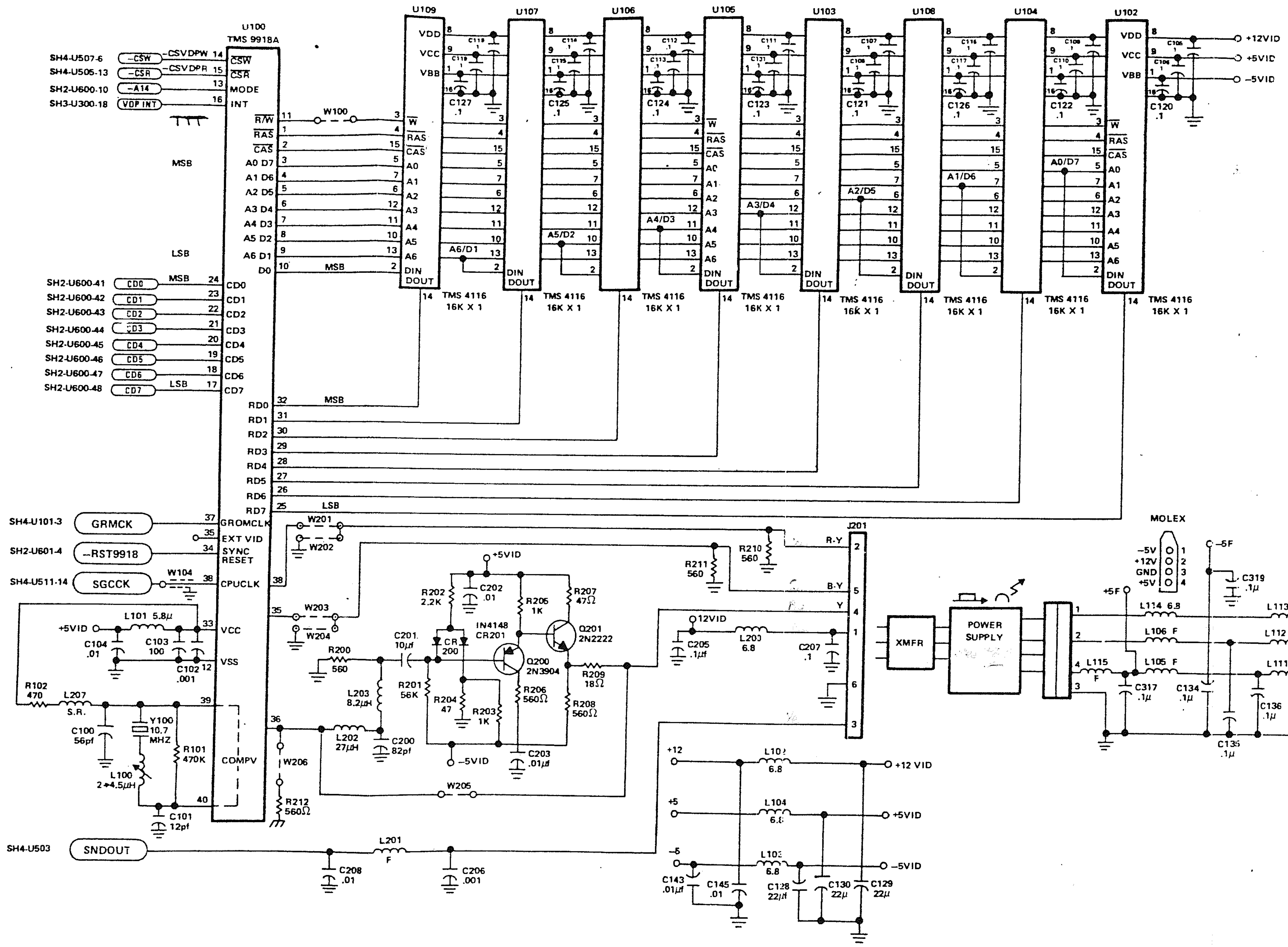
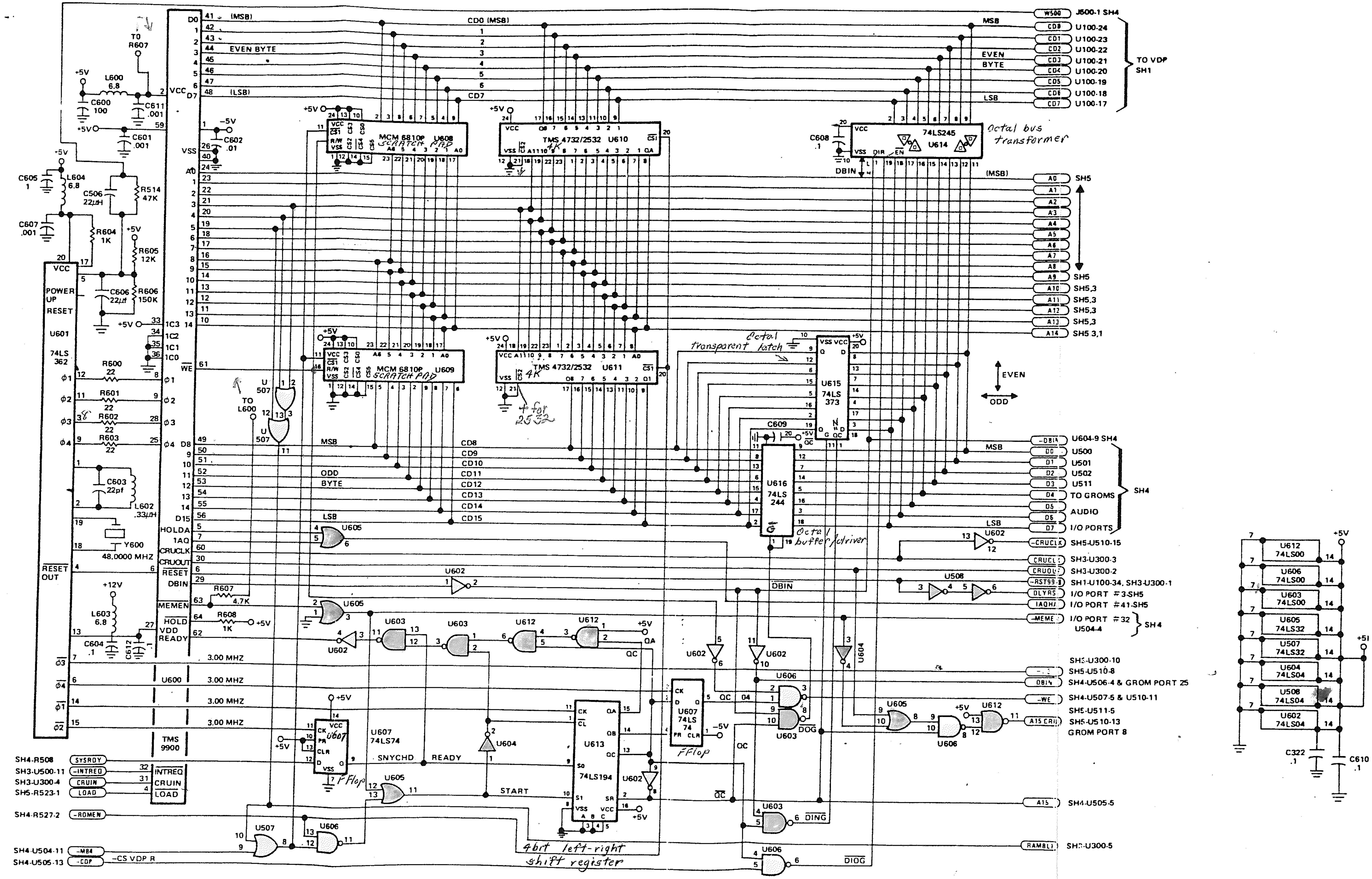


FIGURE E. CONNECTOR PIN IDENTIFICATION DIAGRAM

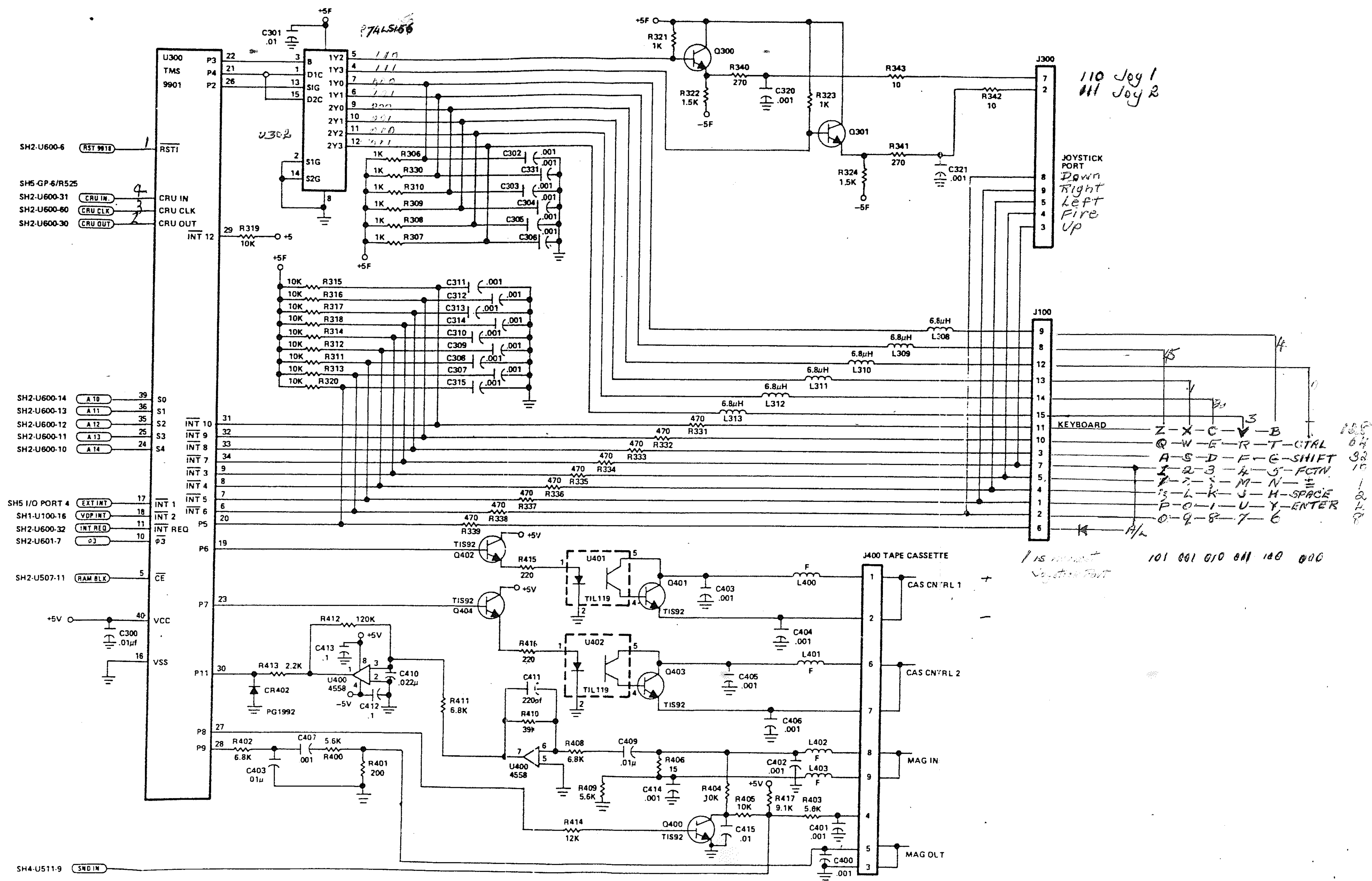


TI-99/4A SCHEMATIC DIAGRAM

(a) VDP/MEMORY 9918A & 4116A
(b) VIDEO & AUDIO OUTPUTS

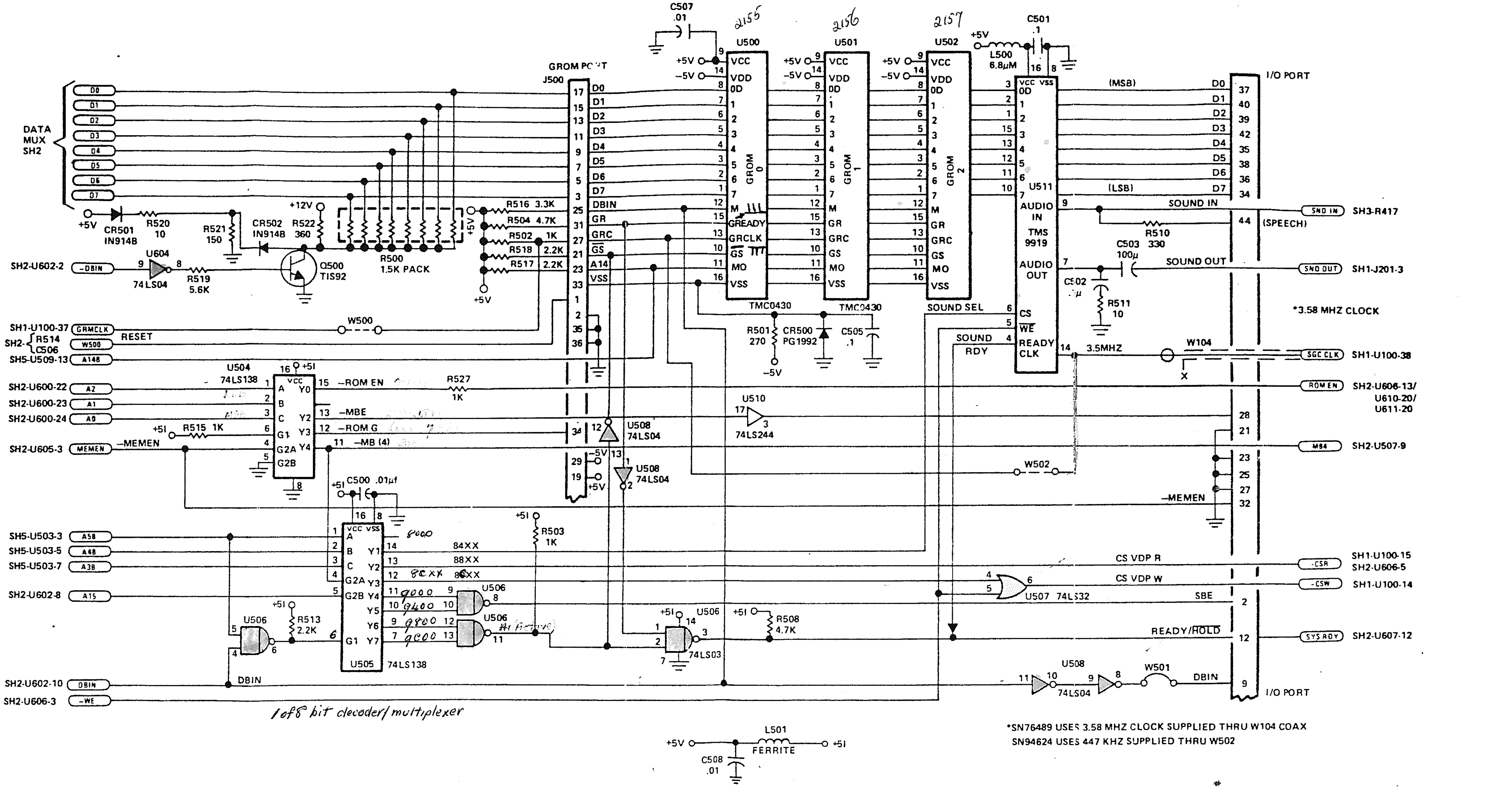


TI-99/4A SCHEMATIC DIAGRAM
CPU 9900



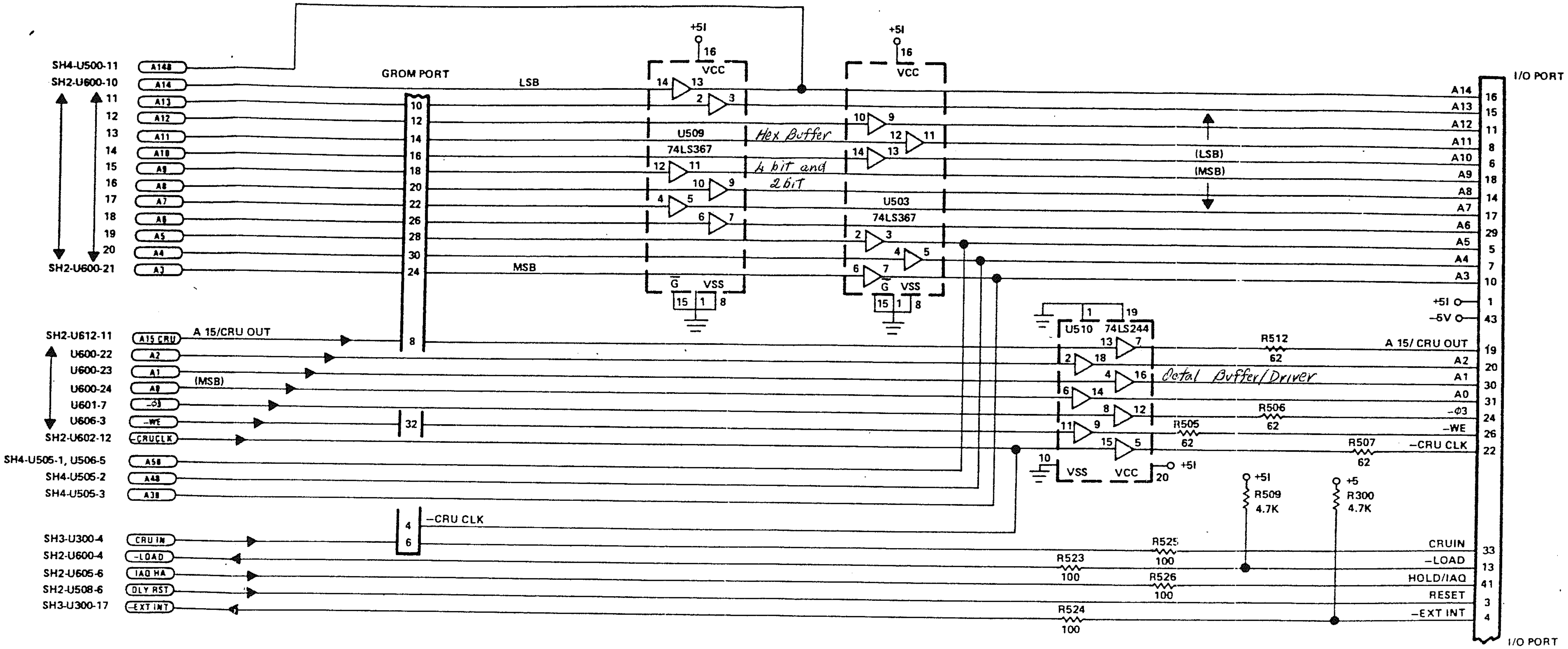
TI-99/4A SCHEMATIC DIAGRAM

CRU 9901



TI-99/4A SCHEMATIC DIAGRAM

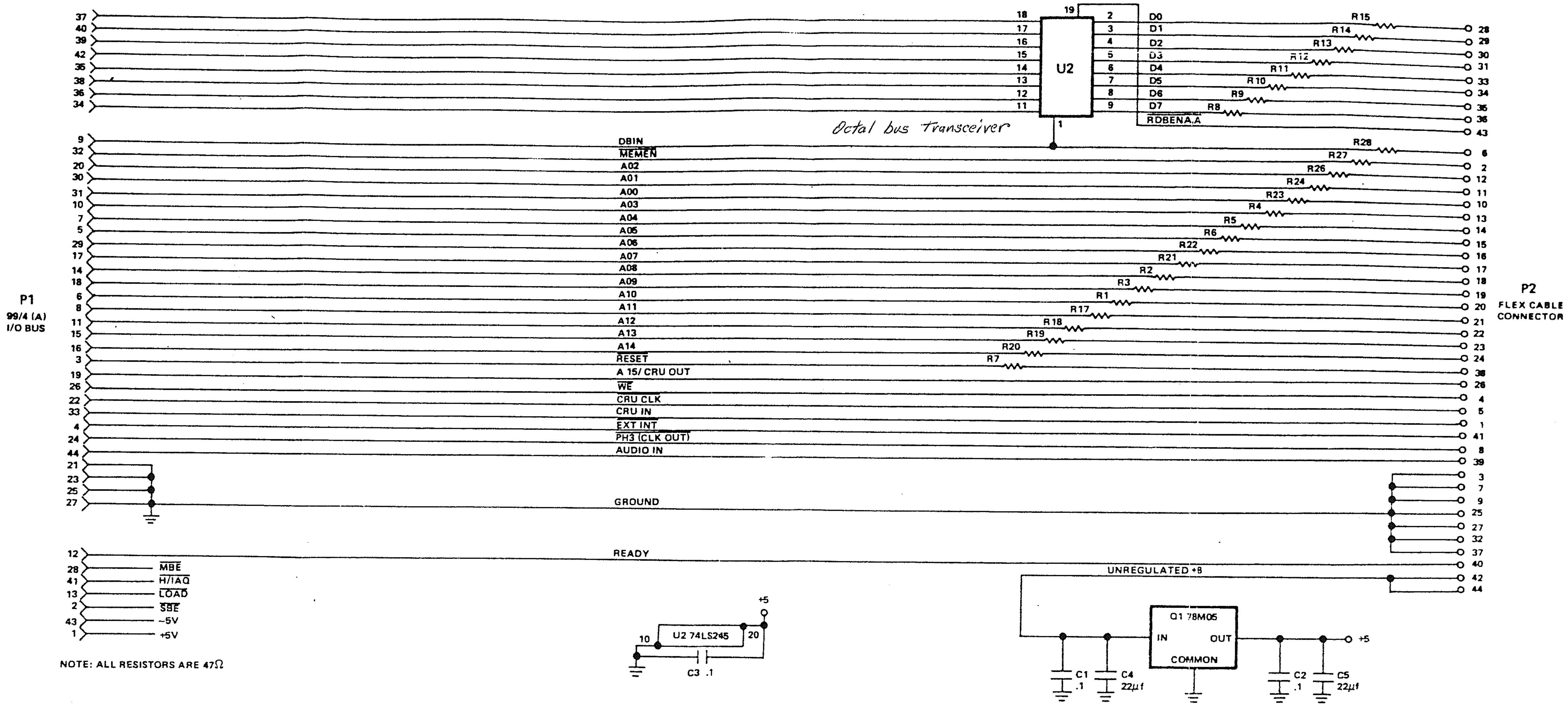
GROM 0430
AUDIO 9919



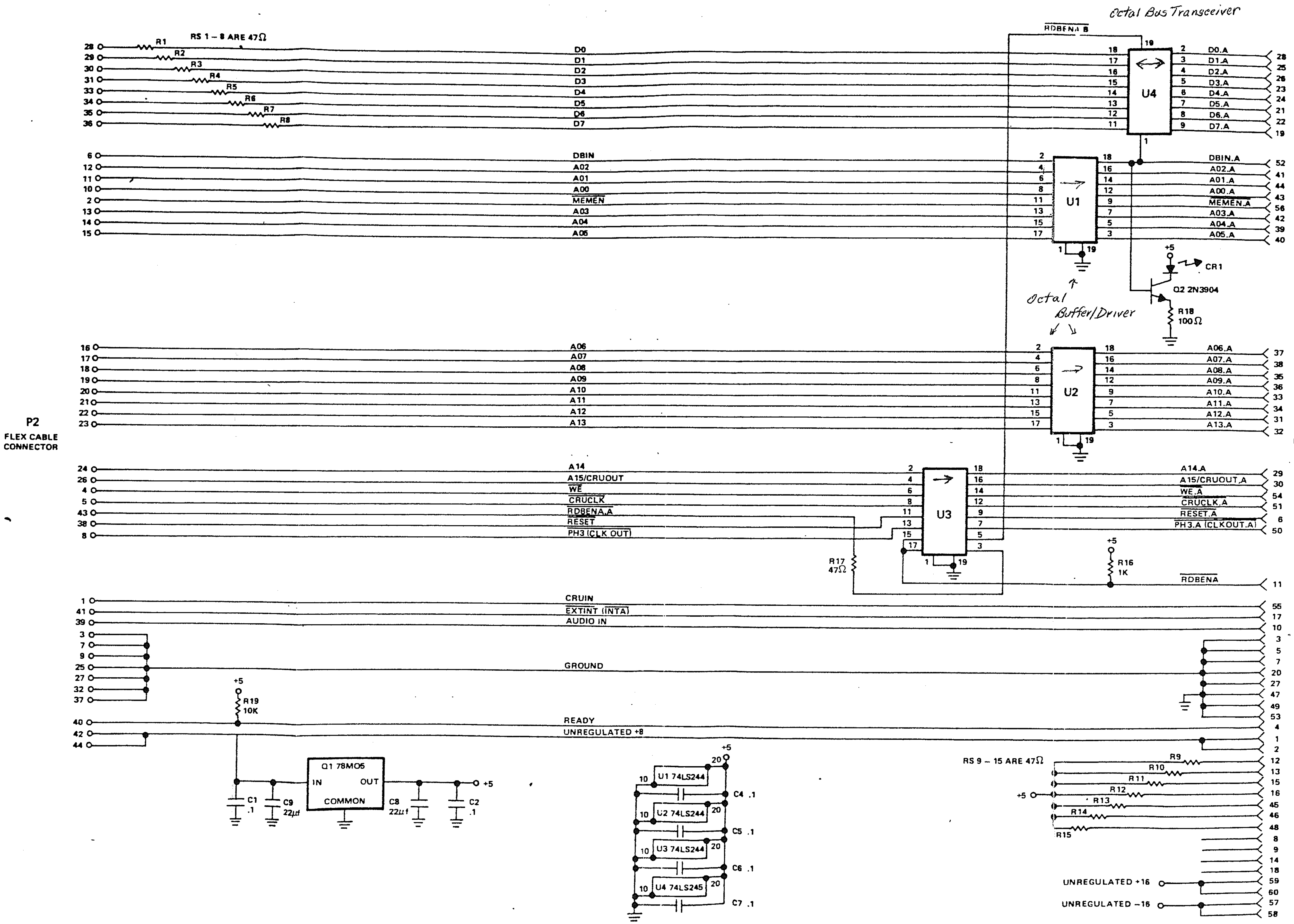
TI-99/4A SCHEMATIC DIAGRAM

GROM PORT
I/O PORT
& BUFFERS

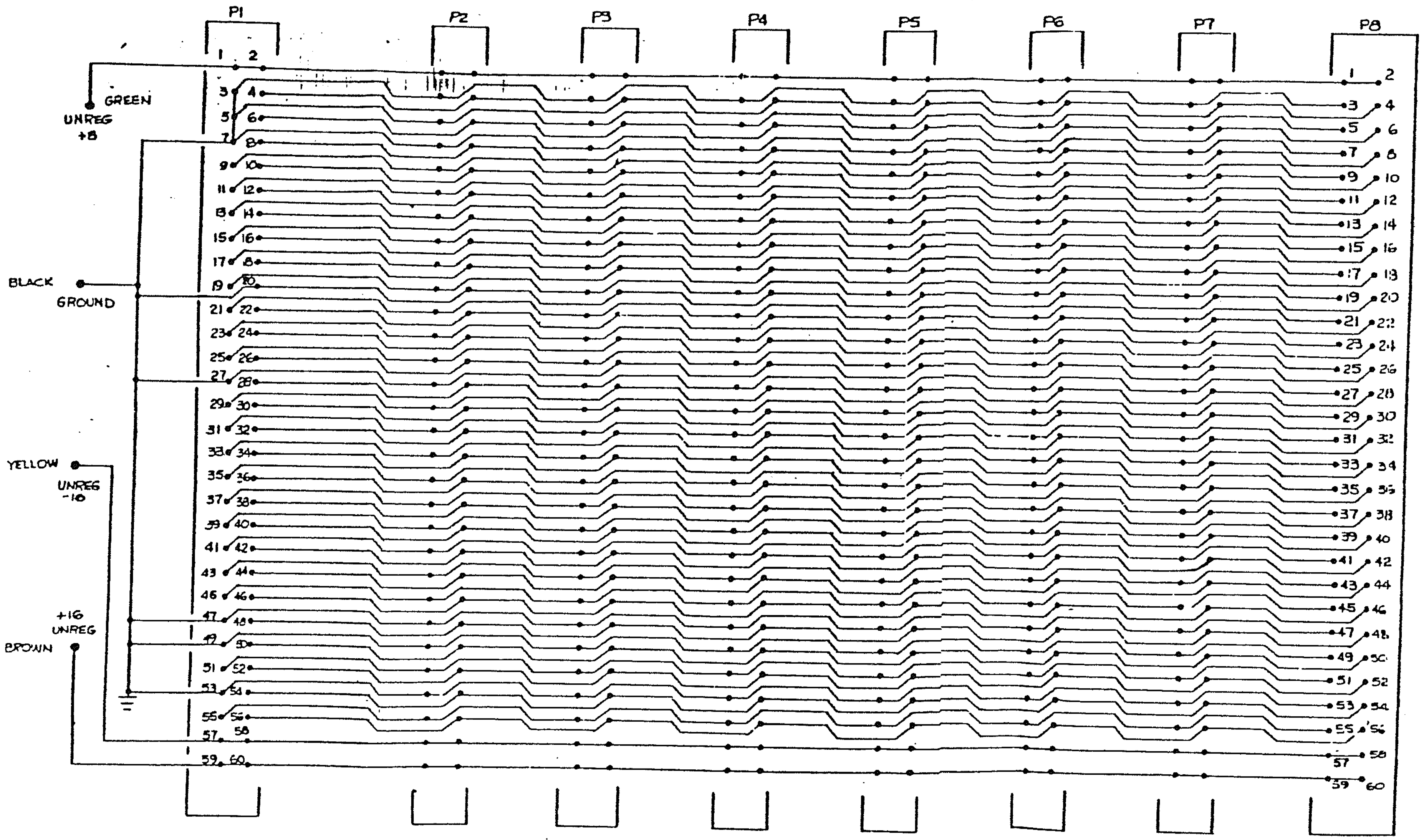
5



FLEX CABLE SCHEMATIC DIAGRAM
'CONSOLE END OF CABLE'



FLEX CABLE SCHEMATIC DIAGRAM
(PERIPHERAL EXPANSION UNIT END OF CABLE)



PERIPHERAL
PERIPHERAL BACK PLANE

ITEM NO.	PART NUMBER	DESCRIPTION	MATERIAL

PARTS LIST

DIMENSION IDENT. NUMBER

USED	NOT USED

NEXT ASSY	USED ON
	360

APPLICATION

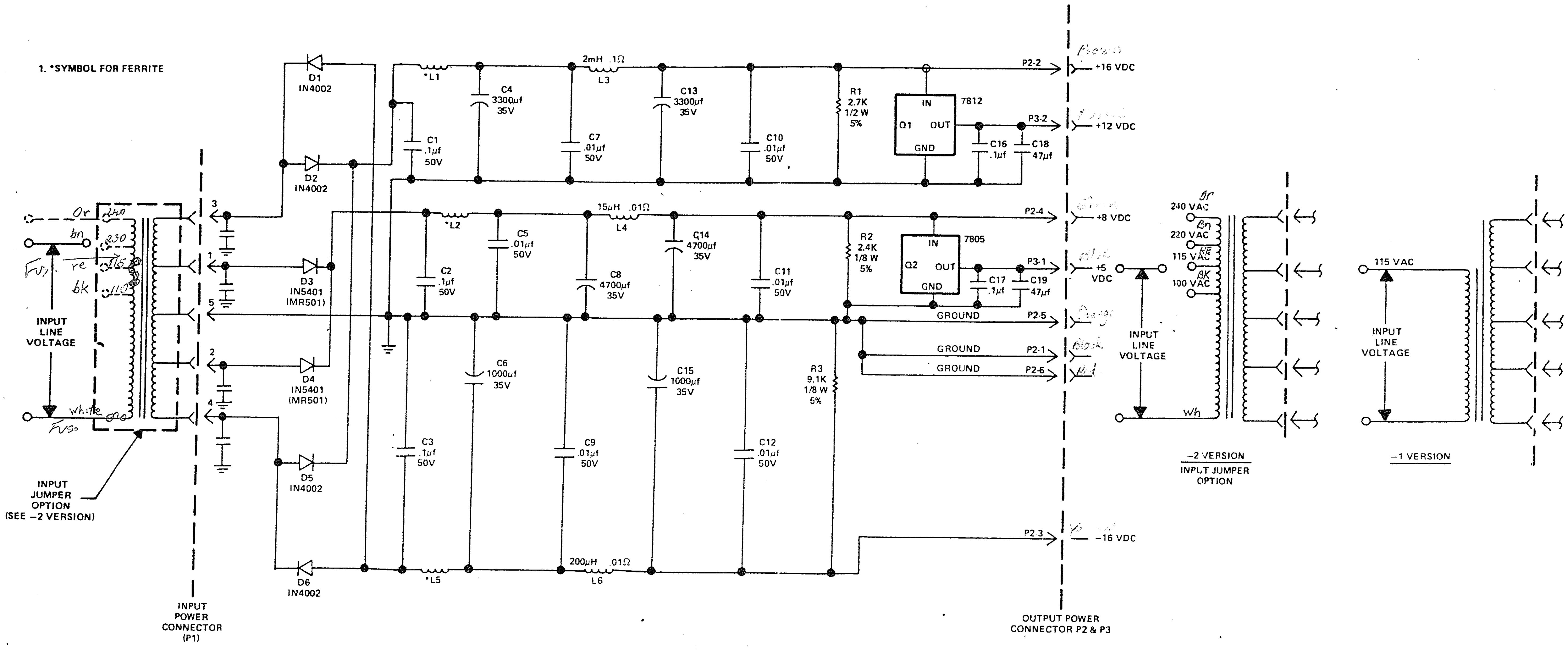
P.Rue 2-17-82

SCHEMATI
PROJECT

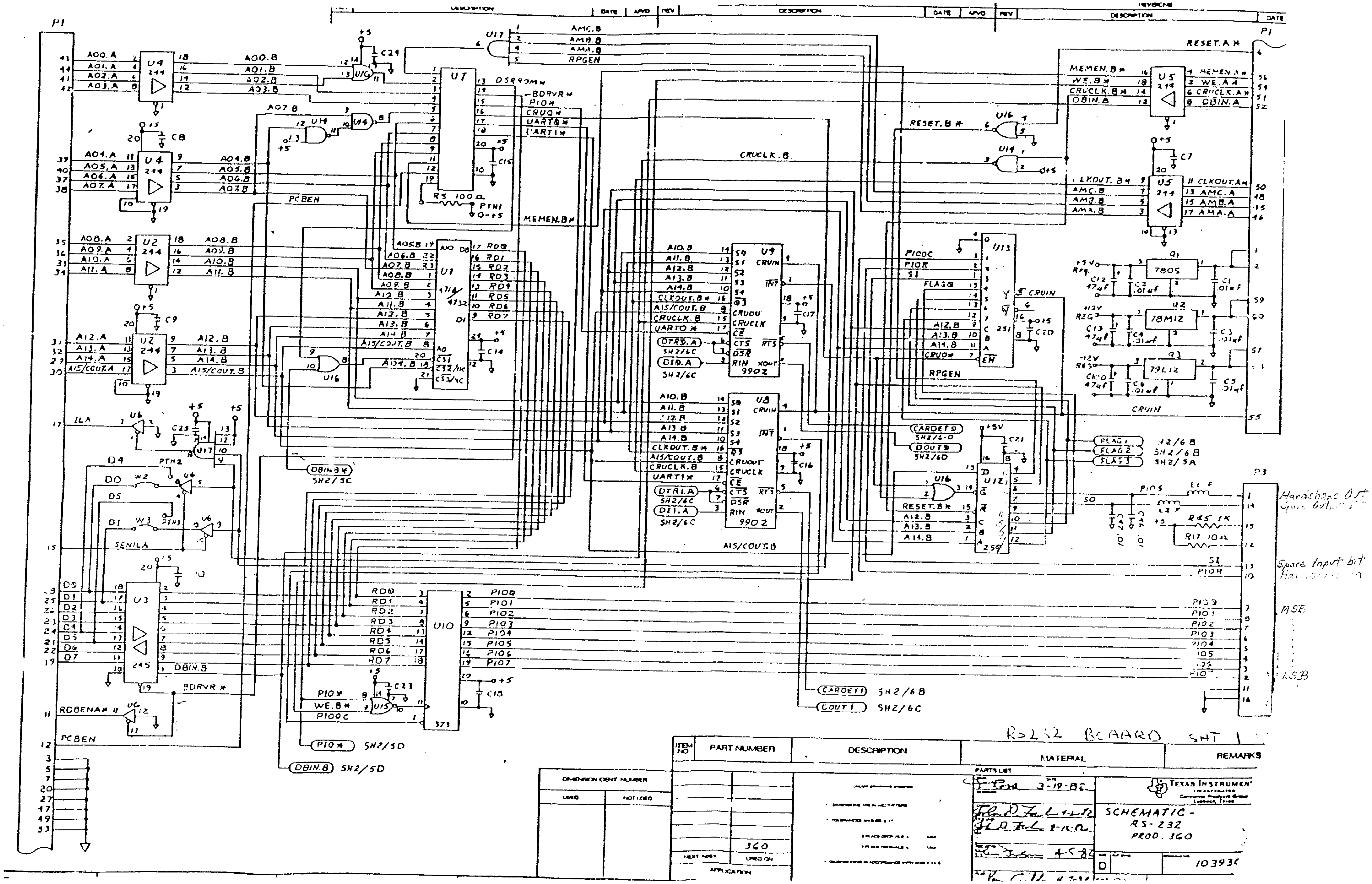
D /

2324004

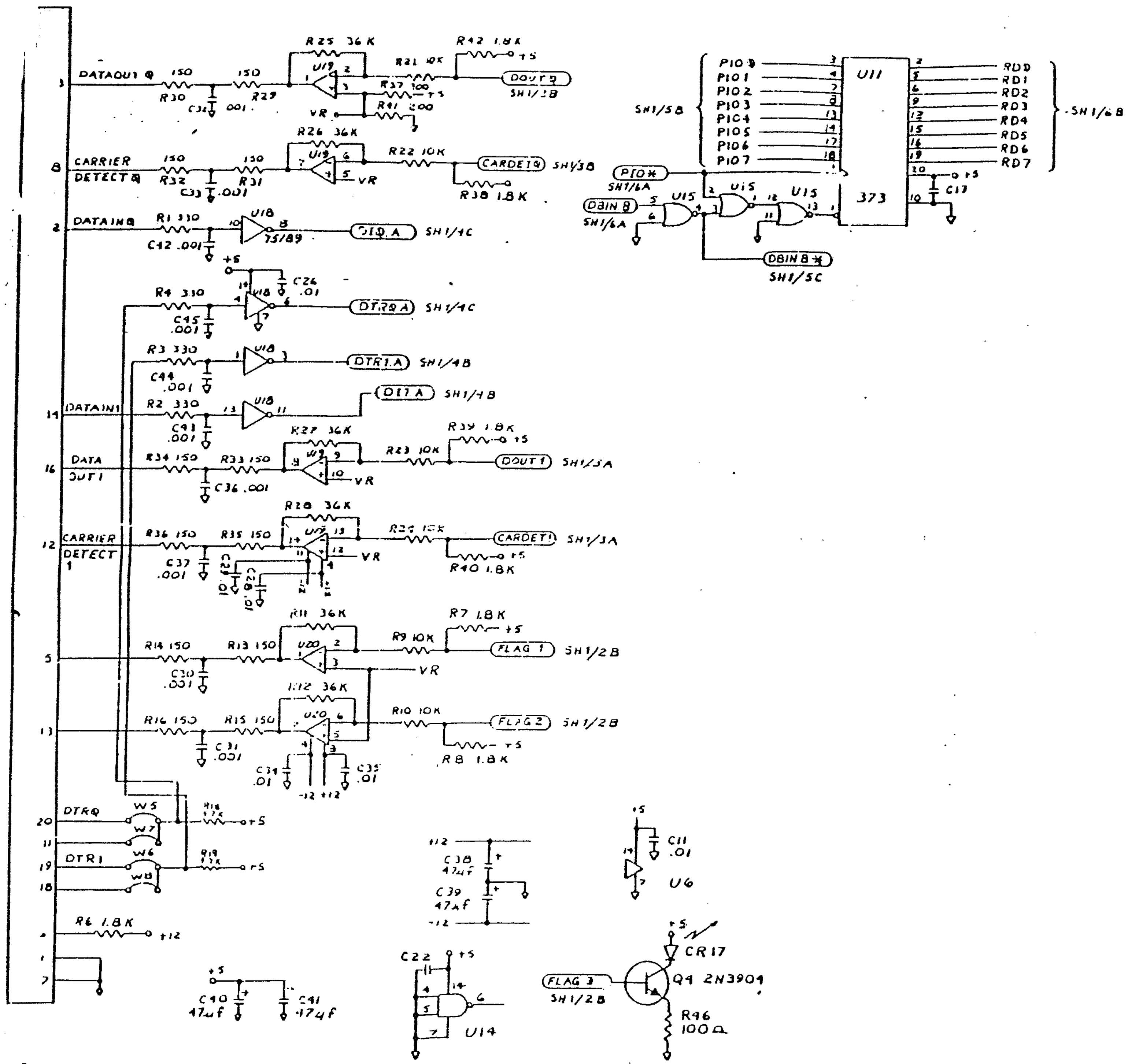
NONE


1. *SYMBOL FOR FERRITE
D1
IN4002
D2
IN4002
D3
IN5401
(MR501)
D4
IN5401
(MR501)
D5
IN4002
D6
IN4002
*L1
*L2
*L5
2mH .1Ω
L3
15μH .01Ω
L4
200μH .01Ω
L6
C1
.1μf
50V
C2
.1μf
50V
C3
.1μf
50V
C4
3300μf
35V
C5
.01μf
50V
C6
1000μf
35V
C7
.01μf
50V
C8
4700μf
35V
C9
.01μf
50V
C10
.01μf
50V
C11
.01μf
50V
C12
.01μf
50V
C13
3300μf
35V
C14
4700μf
35V
C15
1000μf
35V
C16
.1μf
C17
.1μf
C18
47μf
C19
47μf
R1
2.7K
1/2 W
5%
R2
2.4K
1/8 W
5%
R3
9.1K
1/8 W
5%
IN
Q1
OUT
GND
7812
IN
Q2
OUT
GND
7805
P2-2
+16 VDC
P3-2
+12 VDC
P2-4
+8 VDC
P3-1
+5
VDC
GROUND
P2-5
GROUND
P2-1
GROUND
P2-6
P2-3
-16 VDC
INPUT
LINE
VOLTAGE
INPUT
JUMPER
OPTION
(SEE -2 VERSION)
INPUT
POWER
CONNECTOR
(P1)
OUTPUT POWER
CONNECTOR P2 & P3
240 VAC
220 VAC
115 VAC
100 VAC
INPUT
LINE
VOLTAGE
-2 VERSION
INPUT JUMPER
OPTION
115 VAC
INPUT
LINE
VOLTAGE
-1 VERSION

Also see P32



RS232 CARD SHT 1.



RS232 CARD SHT2

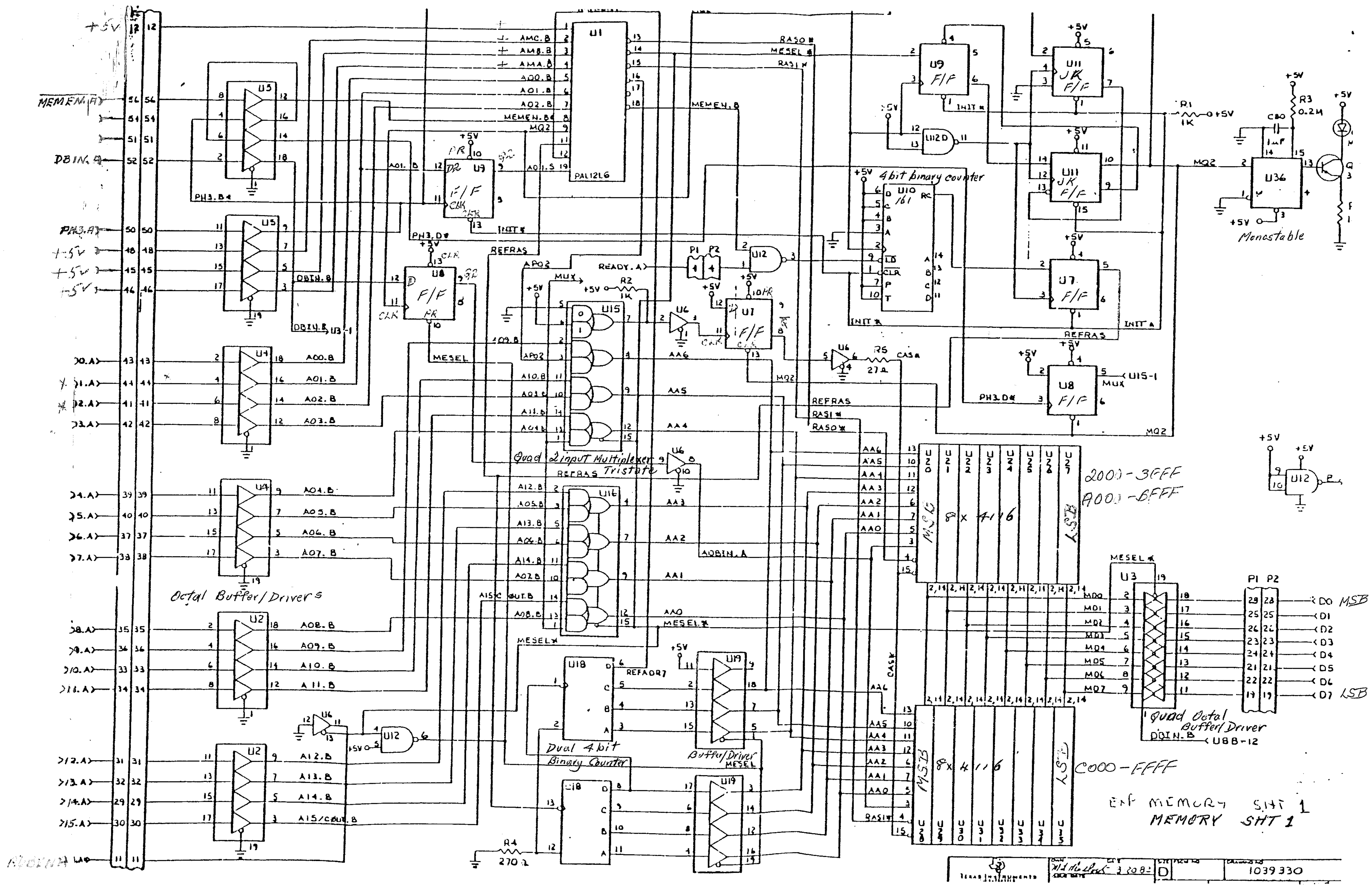
RS232 BOARD SHT2

TEXAS INSTRUMENTS

3-19-82

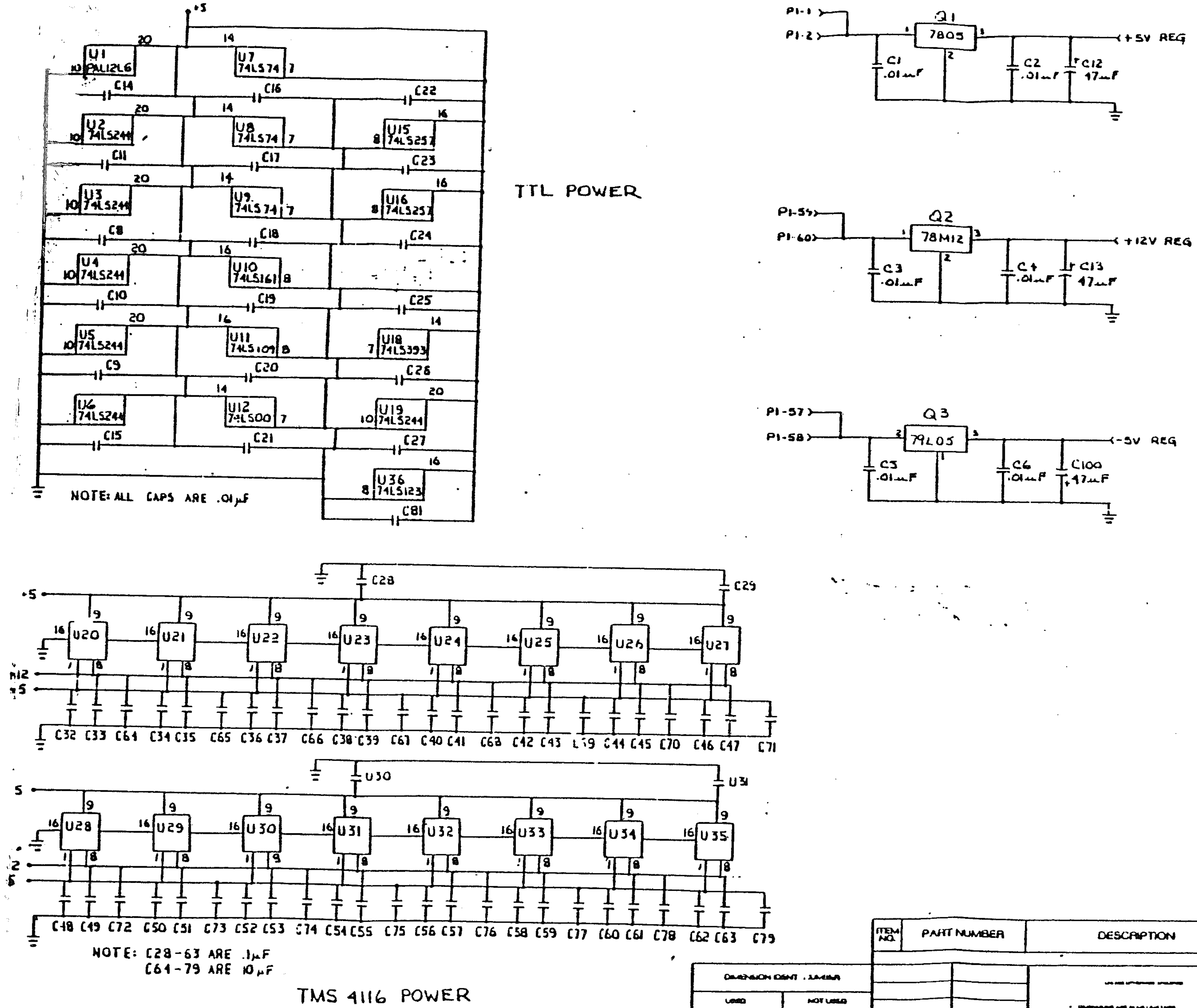
D

1039308



U1
PAL12L6
U9 F/F
U11 JK F/F
U36
Monostable
4 bit binary counter
U10 161
U12
U7 F/F
U8 F/F
U15
Quad 2 input Multiplexer Tristate
U16
Octal Buffer/Drivers
U18
Dual 4 bit Binary Counter
Buffer/Driver
U19
U3
Quad Octal Buffer/Driver
MSB 8 x 4116 LSB
2000-3FFF
A000-BFFF
C000-FFFF
EXP MEMORY SHT 1
MEMORY SHT 1
D0 MSB
D7 LSB
MEMEN.A
DBIN.A
PH3.A
ADBIN.A
1039330
D

REV	DESCRIPTION	DATE	APVD
A	NO ECN - M L Medlock 3-22-82 REDREW SCHEMATIC.		
	FORMAL RELEASE		
B	ECN 102986 ... 7-6-82 1) CHANGED U1 TO A PAL12L6	9/1/82	P.R.



EXPANSION MEMORY SHT 2 Power

ITEM NO.	PART NUMBER	DESCRIPTION	MATERIAL	REMARKS

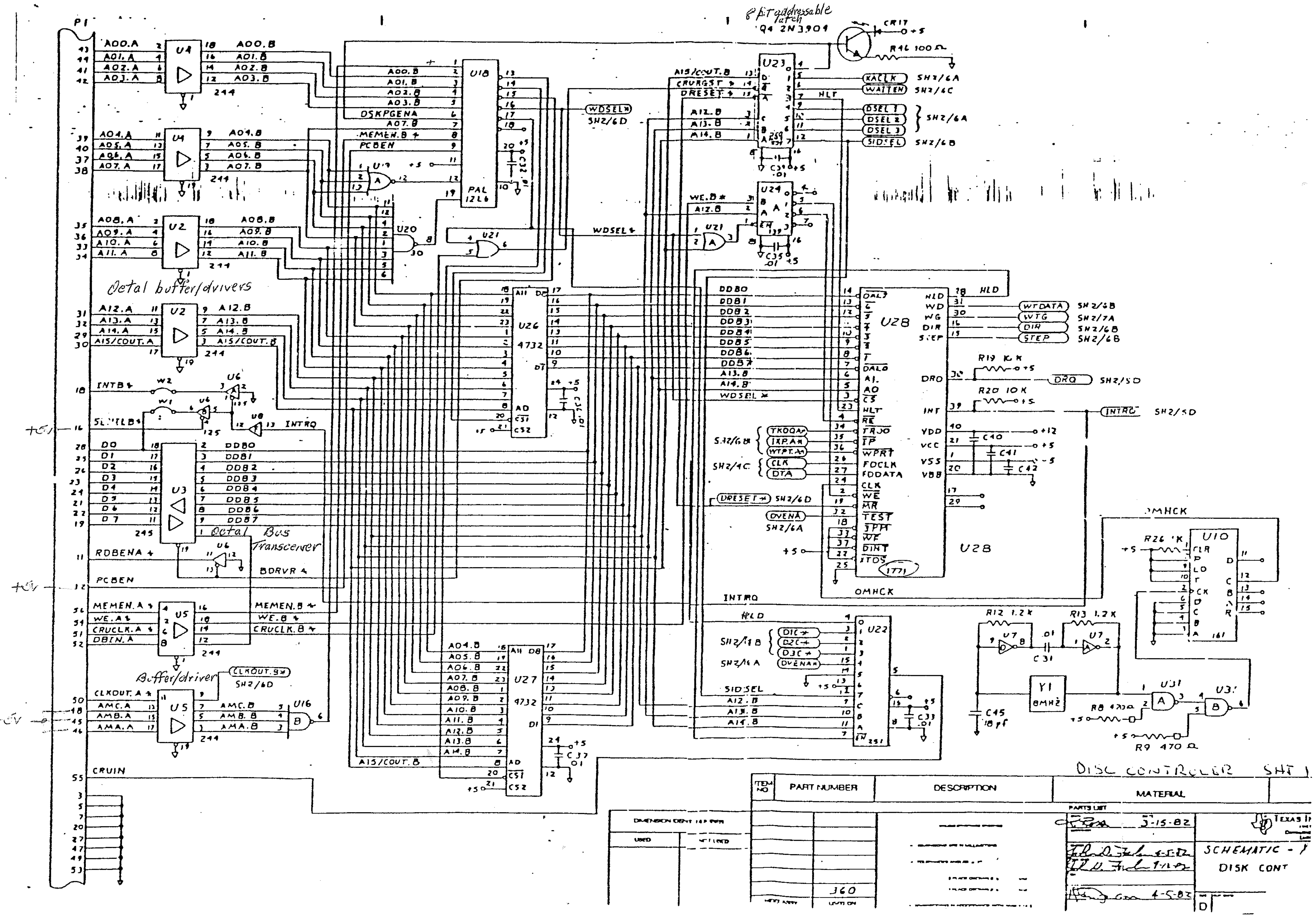
NEXT ASSY	360
APPLICATION	

TEXAS INSTRUMENTS

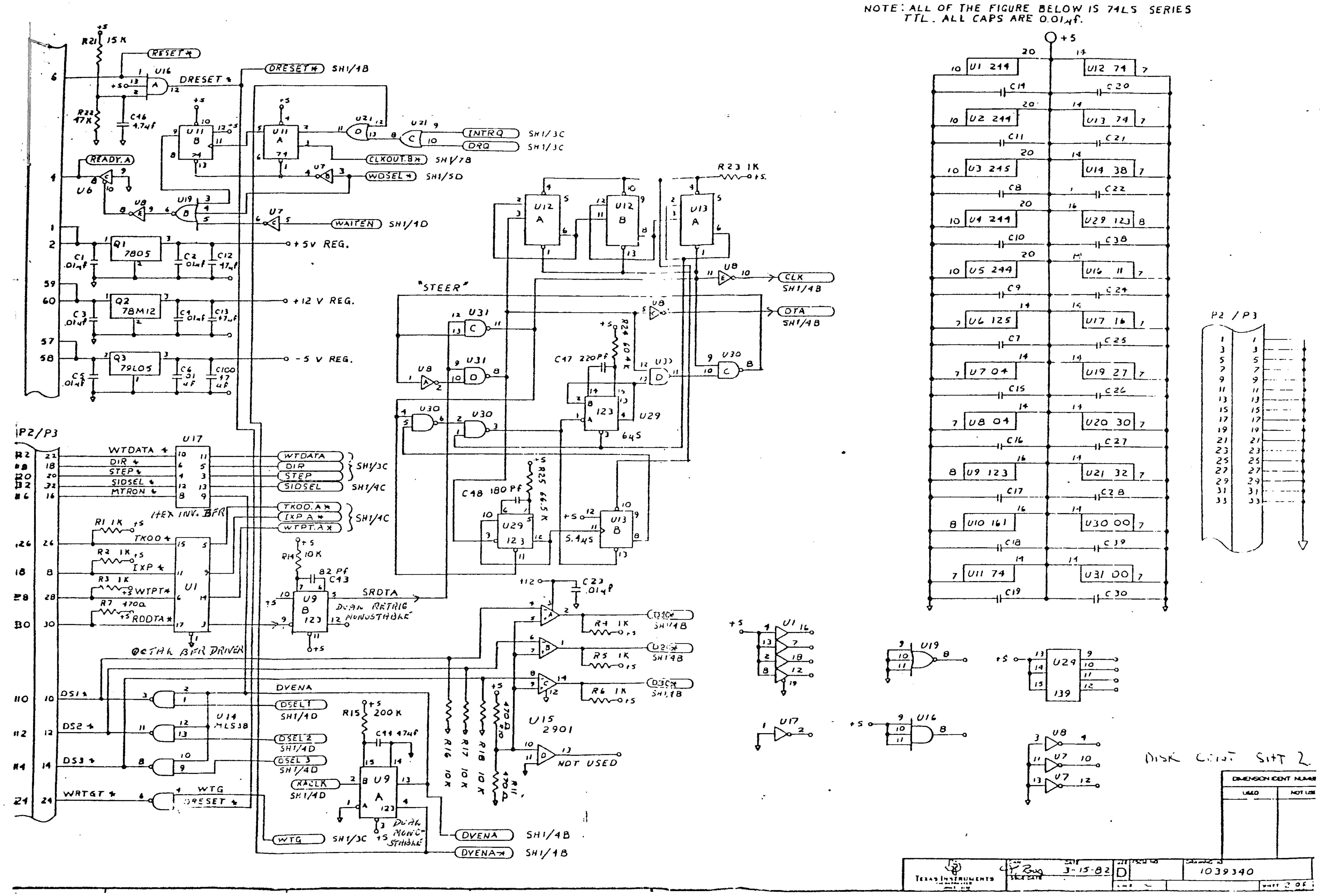
SCHEMATIC PCB
PROJ. 360
MEMORY EXPAN. - JOHNNY B(

M L Medlock 3-22-82

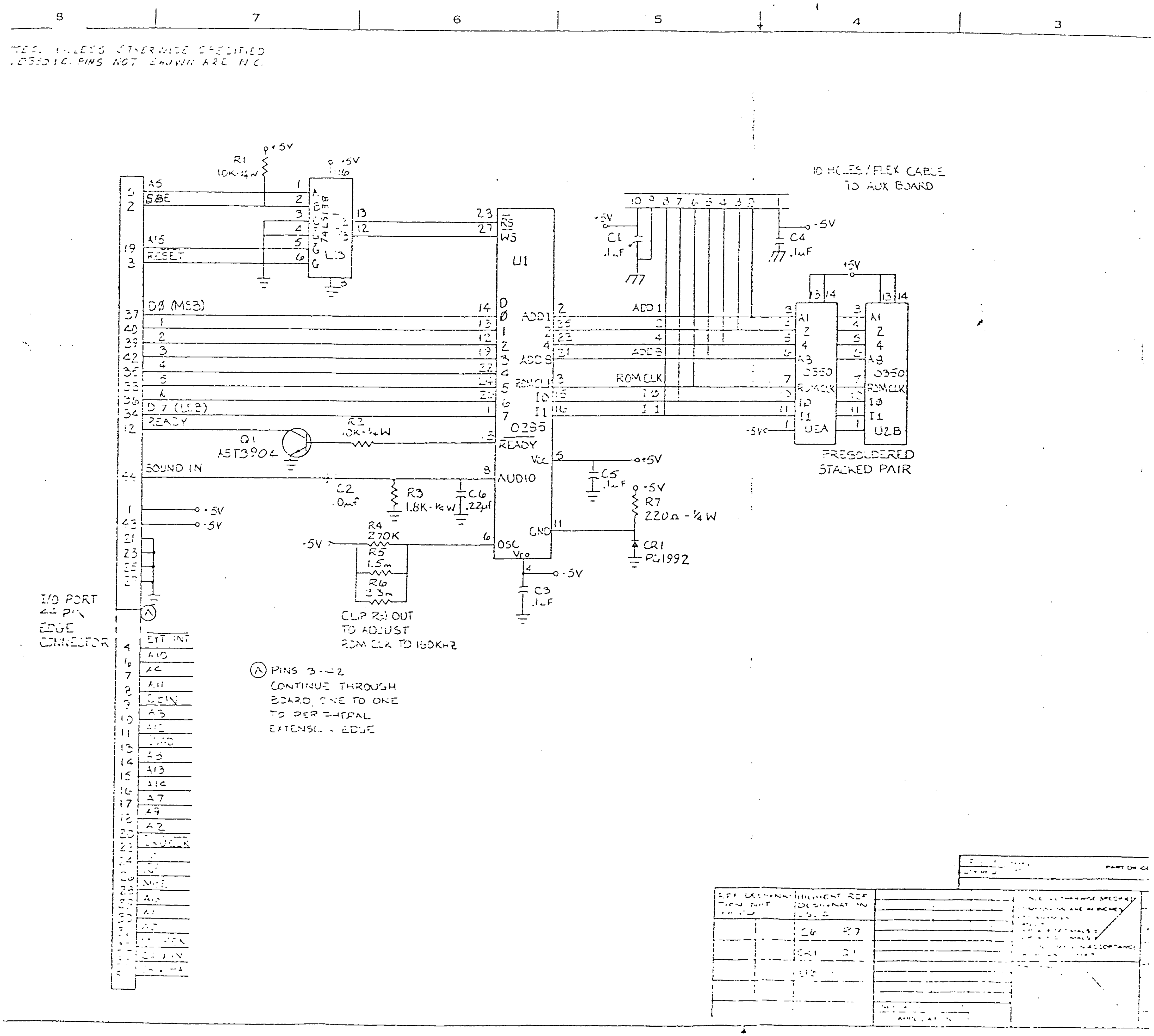
D 1039330

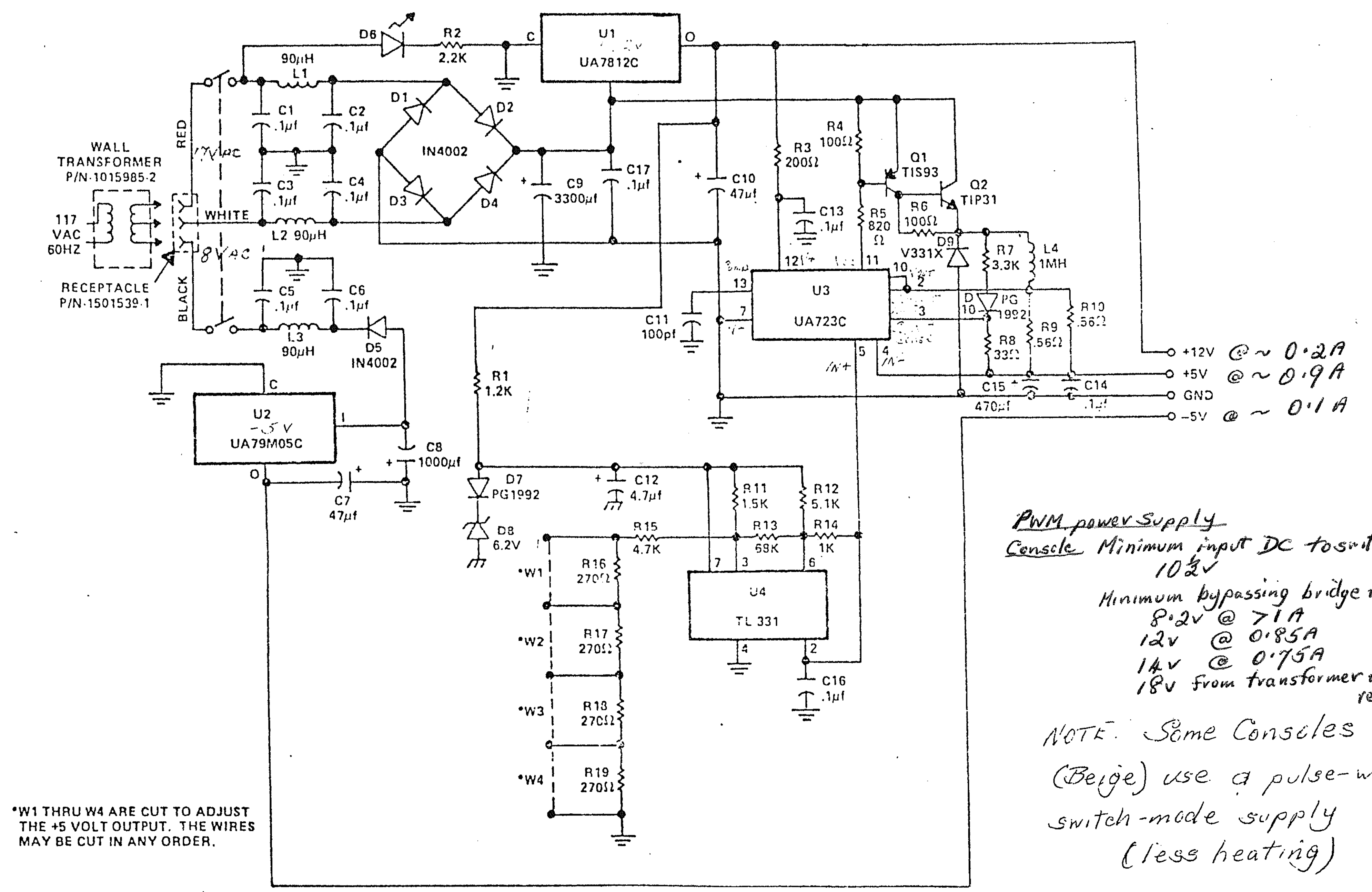


DISK CONTROLLER SHT 1



DISK CONTROLLER SHT 2

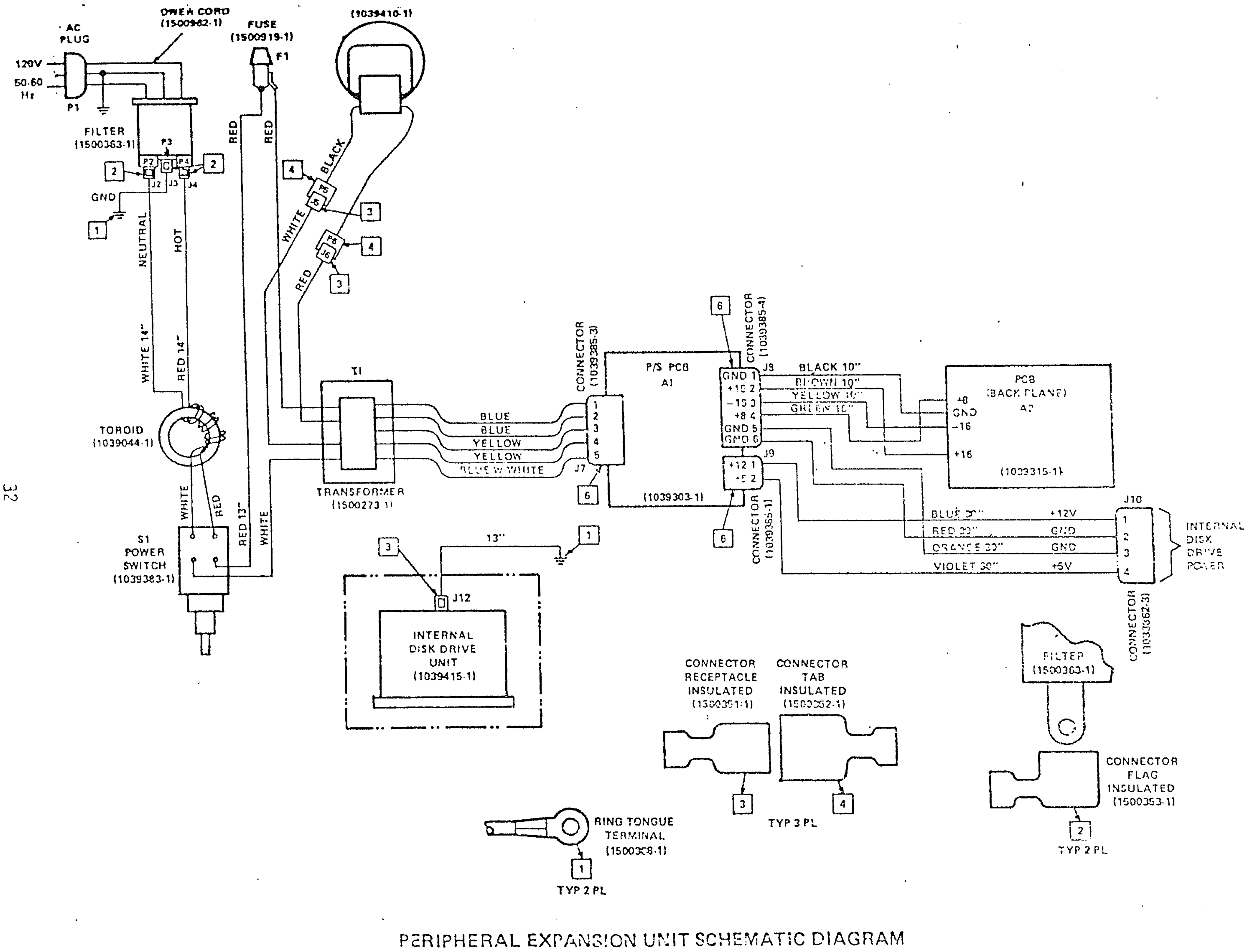

8
7
6
5
4
3
R1
10K-¼W
+5V
74LS138
U3
U1
0285
D0 (MSB)
D7 (LSB)
READY
Q1
A5T3904
R2
10K-¼W
SOUND IN
AUDIO
C2
R3
1.8K-¼W
C6
.22µf
R4
270K
R5
1.5m
R6
3.3m
-5V
OSC
GND
C3
.1µF
C5
.1µF
R7
220Ω - ¼W
CR1
PG1992
ADD 1
ADD 8
ROM CLK
10 HOLES / FLEX CABLE
TO AUX BOARD
C1
.1µF
C4
.1µF
0350
U2A
U2B
PRESOLDERED
STACKED PAIR
I/O PORT
44 PIN
EDGE
CONNECTOR
CLIP R5 OUT
TO ADJUST
ROM CLK TO 160KHZ
(A) PINS 3-42
CONTINUE THROUGH
BOARD, ONE TO ONE
TO PERIPHERAL
EXTENSION EDGE
EXT INT
A10
A11
A3
A13
A14
A7
A2



PWM power supply
Console Minimum input DC to switch 10½V
Minimum bypassing bridge rectifier
8.2V @ >1A
12V @ 0.85A
14V @ 0.75A
18V from transformer & bridge rectifier.

NOTE: Some Consoles (Beige) use a pulse-width switch-mode supply (less heating)

FIGURE G. TI-99/4A CONSOLE POWER SUPPLY



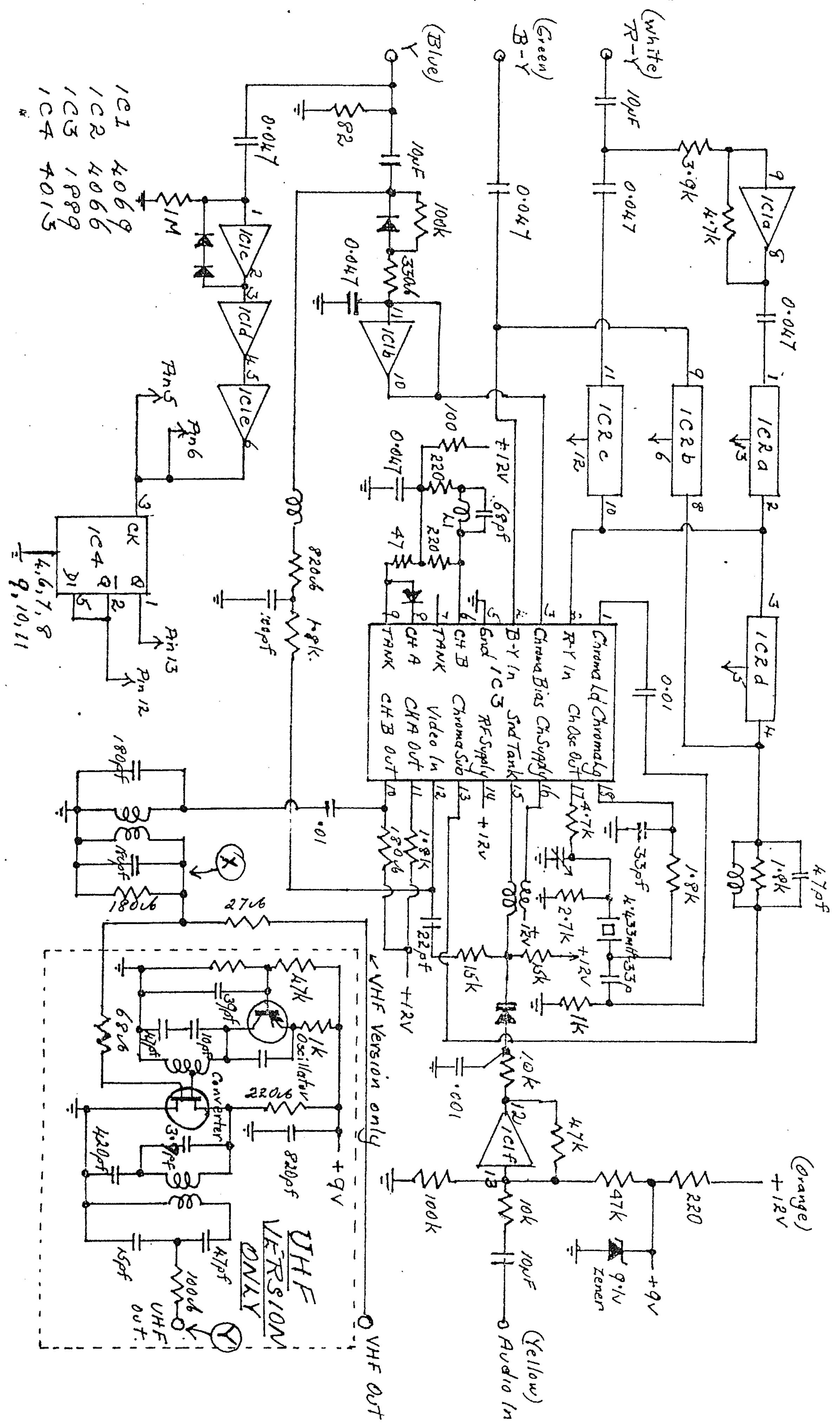
PERIPHERAL EXPANSION UNIT SCHEMATIC DIAGRAM

TI99/4A KEYBOARD WIRING MATRIX

PIN 1 IS NEAREST TO JOYSTICK PORT ON THE MOTHERBOARD.

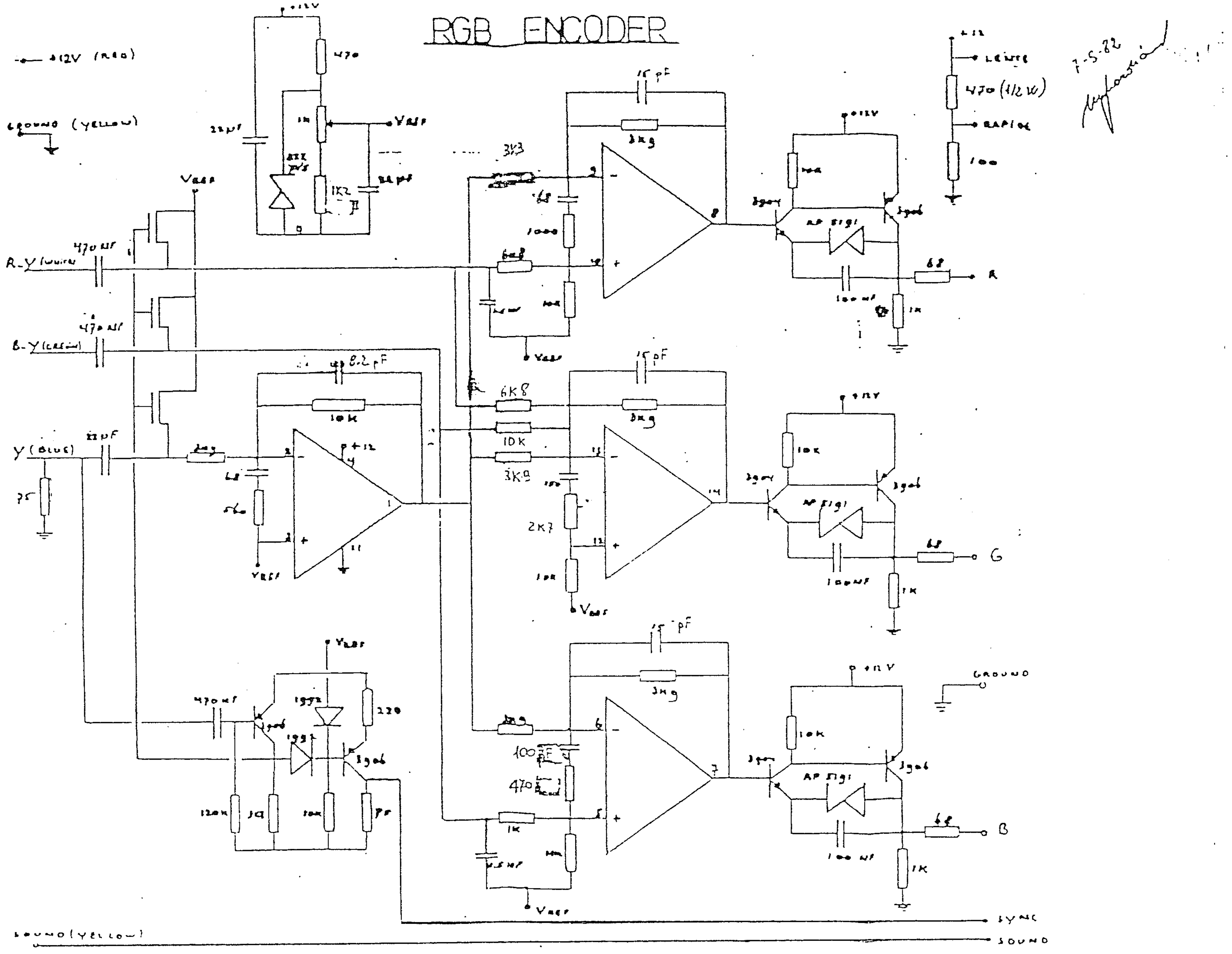
PINS	6	8	13	14	15	9	12
7	AL	1	2	3	4	5	FCTN
10		Q	W	E	R	T	CTRL
3		A	S	D	F	G	SHIFT
11		Z	X	C	V	B	
2		0	9	8	7	6	
1		P	O	I	U	Y	ENTER
4		:	L	K	J	H	SPACE
5		/	>	<	M	N	=

MODULATOR CIRCUIT



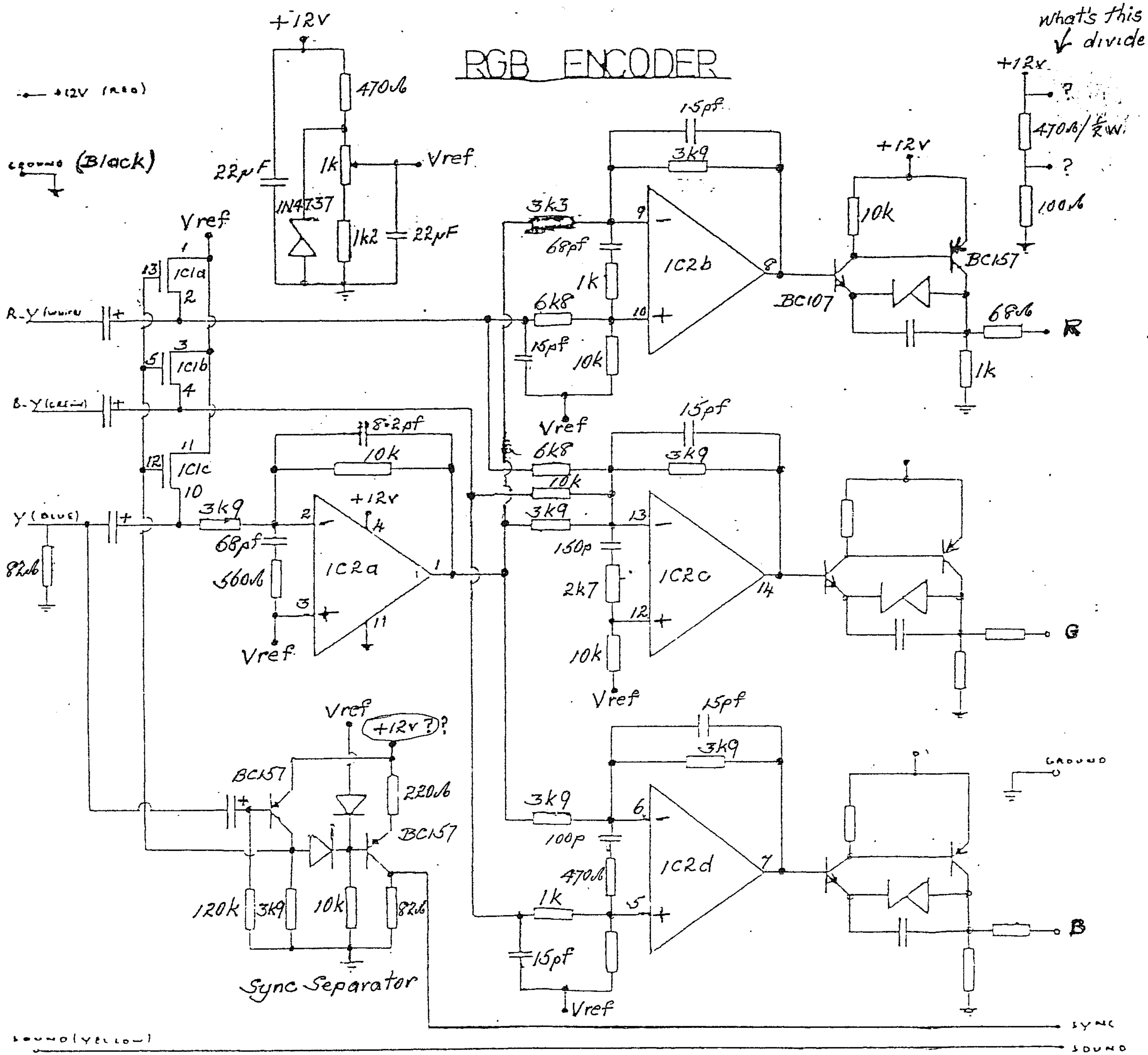
ORIGINAL SUPPLIED BY T.I.

RGB ENCODER



NOTE. Components & values Suggested only

RGB ENCODER



IC1 4066 or 4016

IC2 Same Pinouts as
LM324 1MHz bandwidth Low current.
TL074 3MHz JFET *
LF347 4MHz JFET *
* Preferred.

Zener Diode for Vref circuit. 7.5V
Zener Diodes in R, G & B Buffers probably 5.1V types.

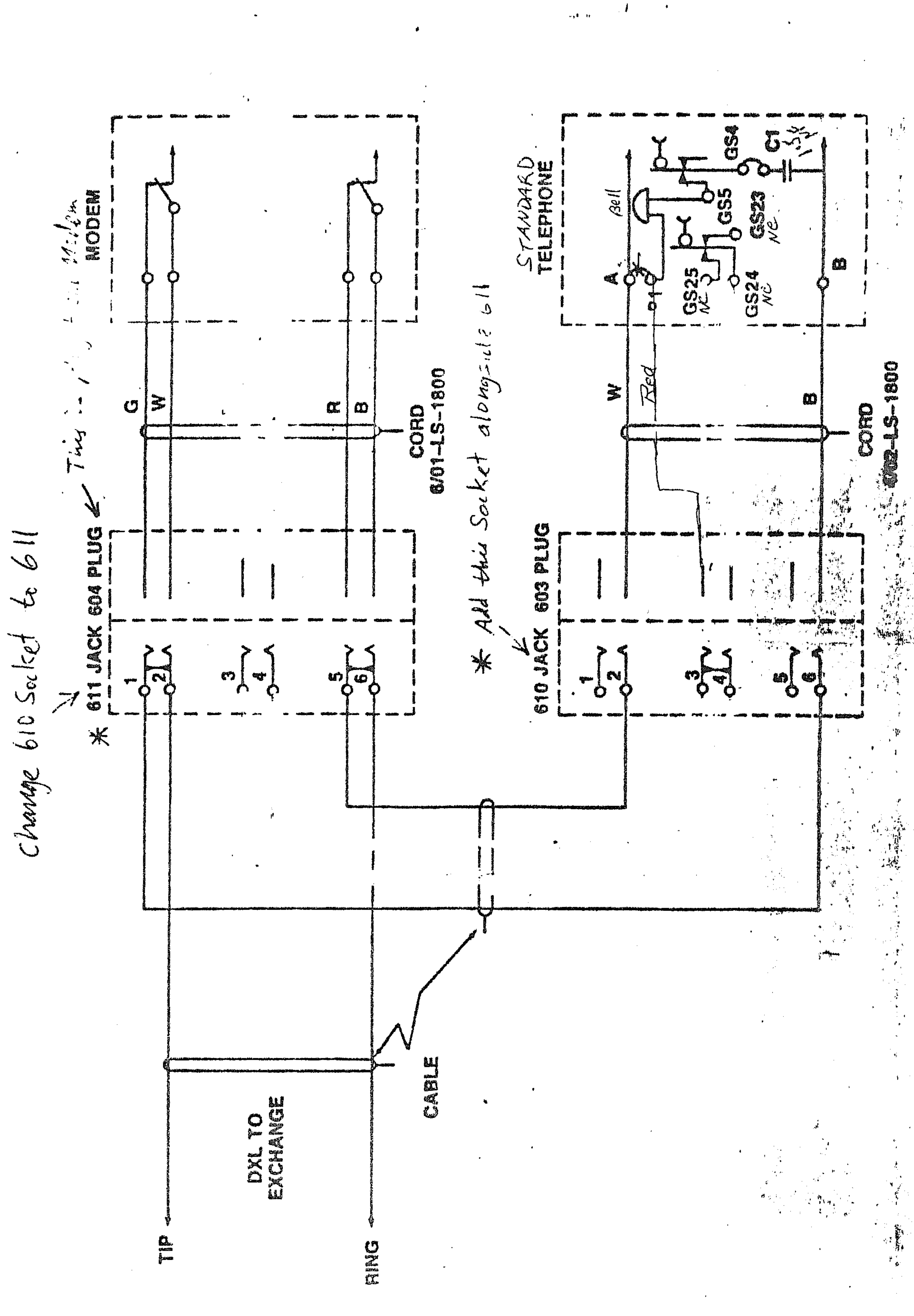
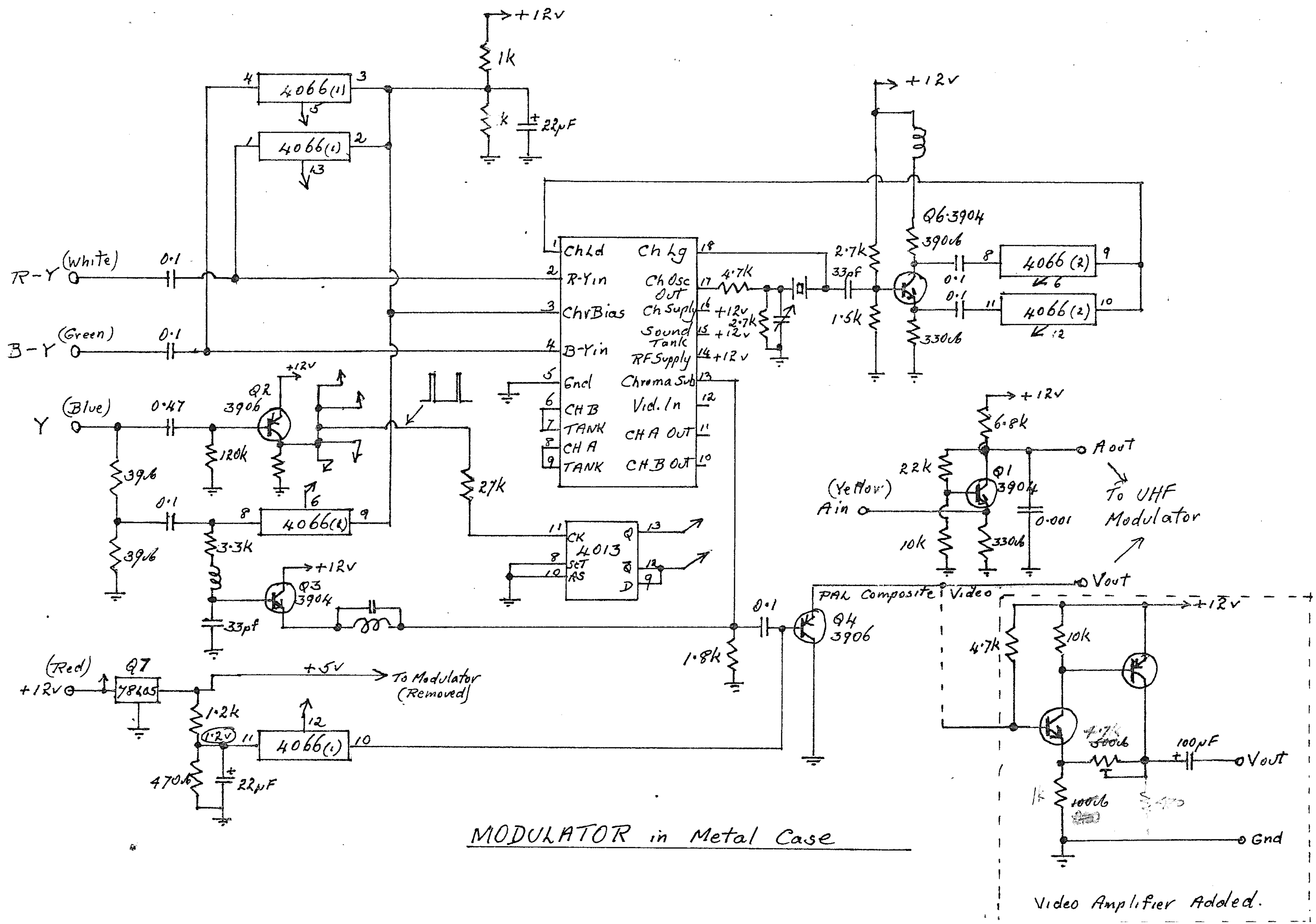


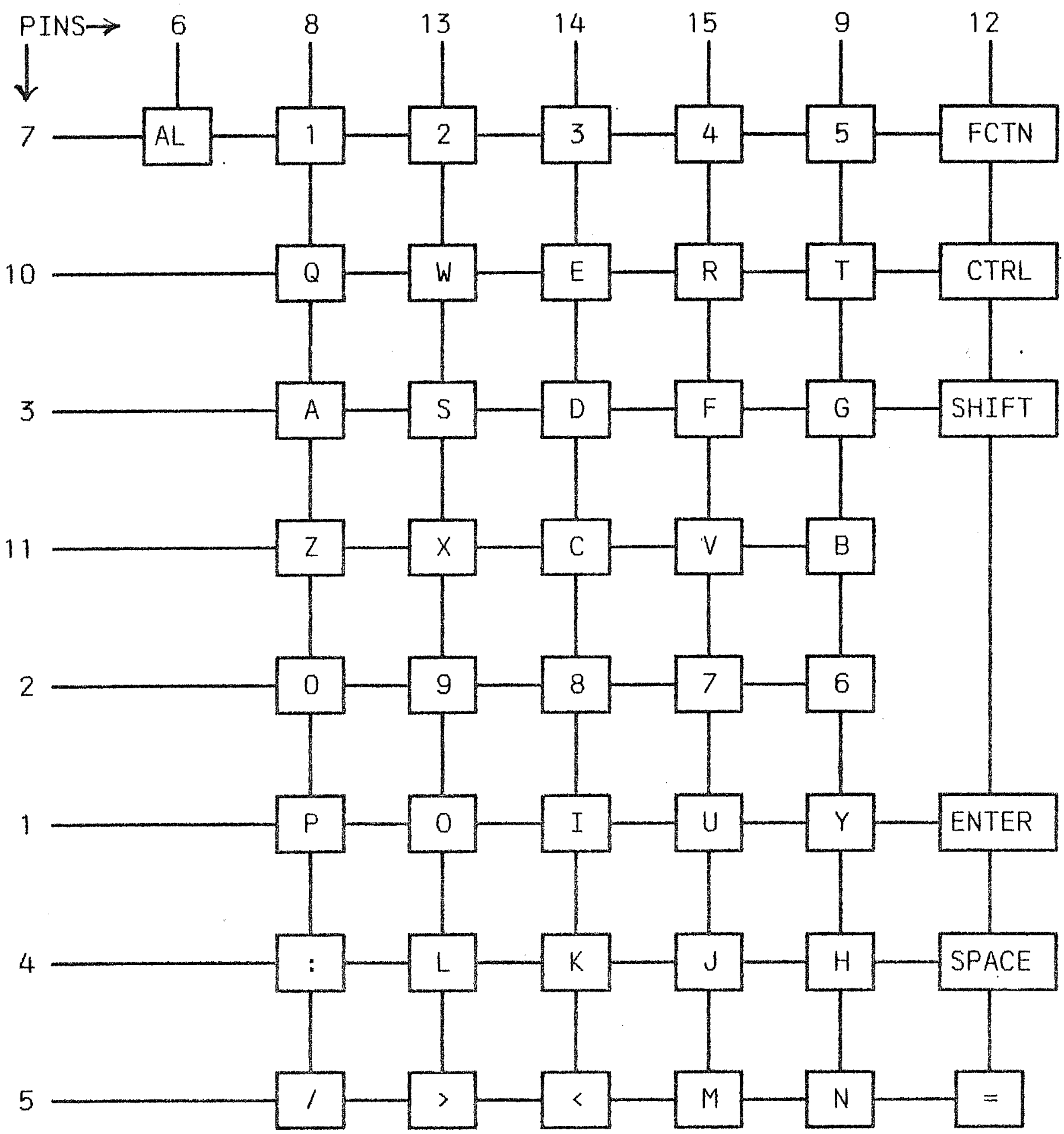
Figure 3-2. Connector Schematic



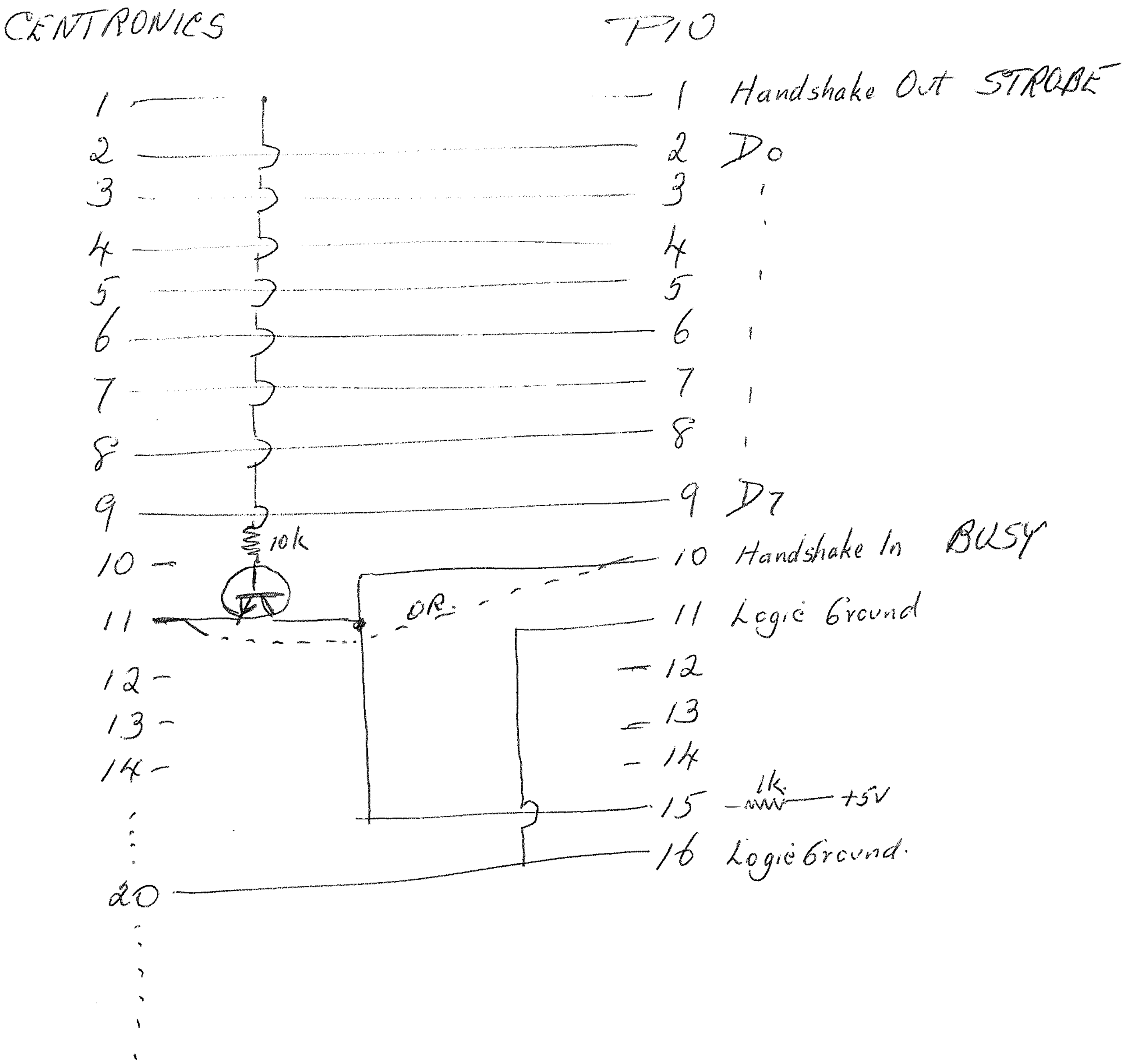
MODULATOR in Metal Case

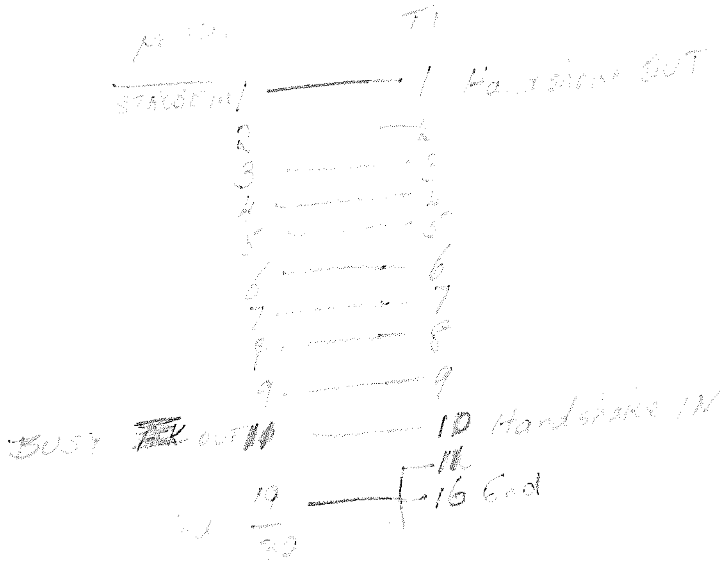
TI99/4A KEYBOARD WIRING MATRIX

PIN 1 IS NEAREST TO JOYSTICK PORT ON THE MOTHERBOARD.

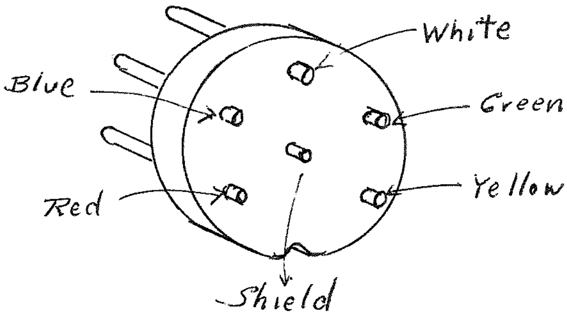


PRINTER CABLE

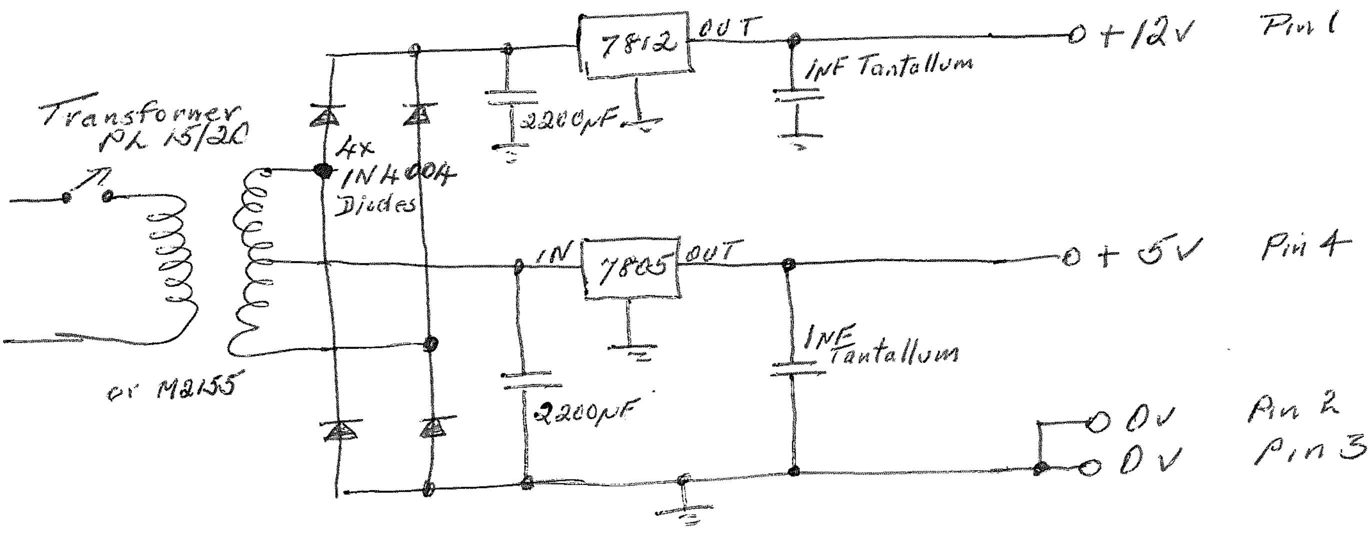


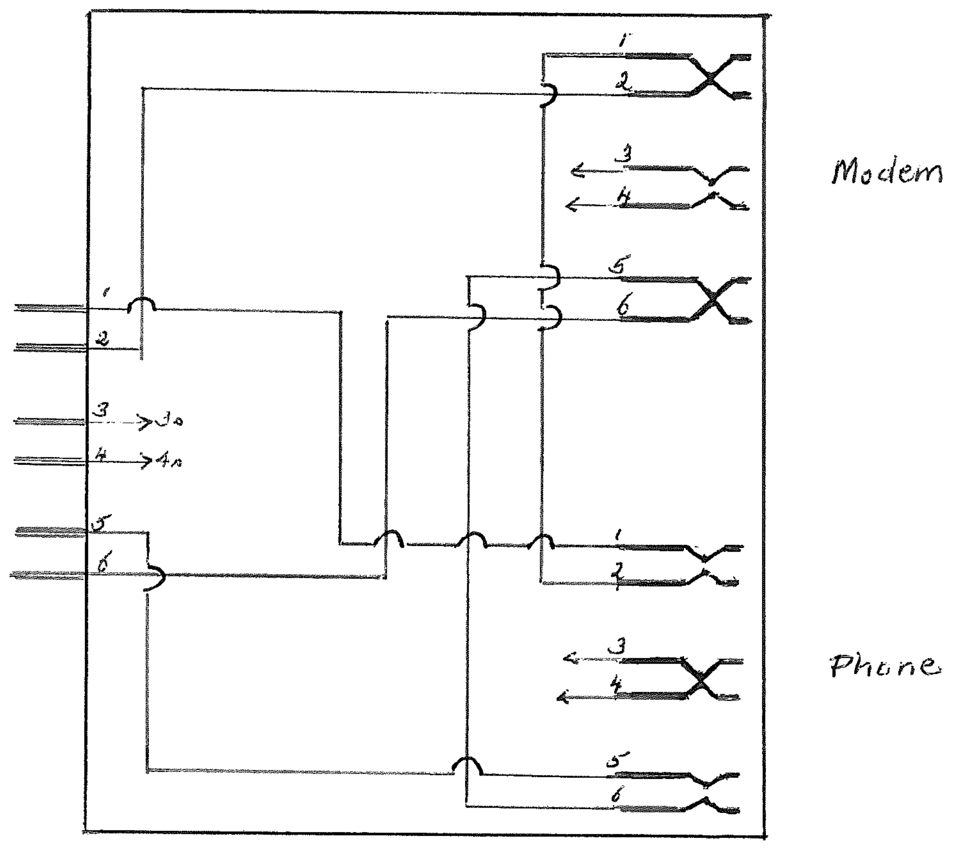


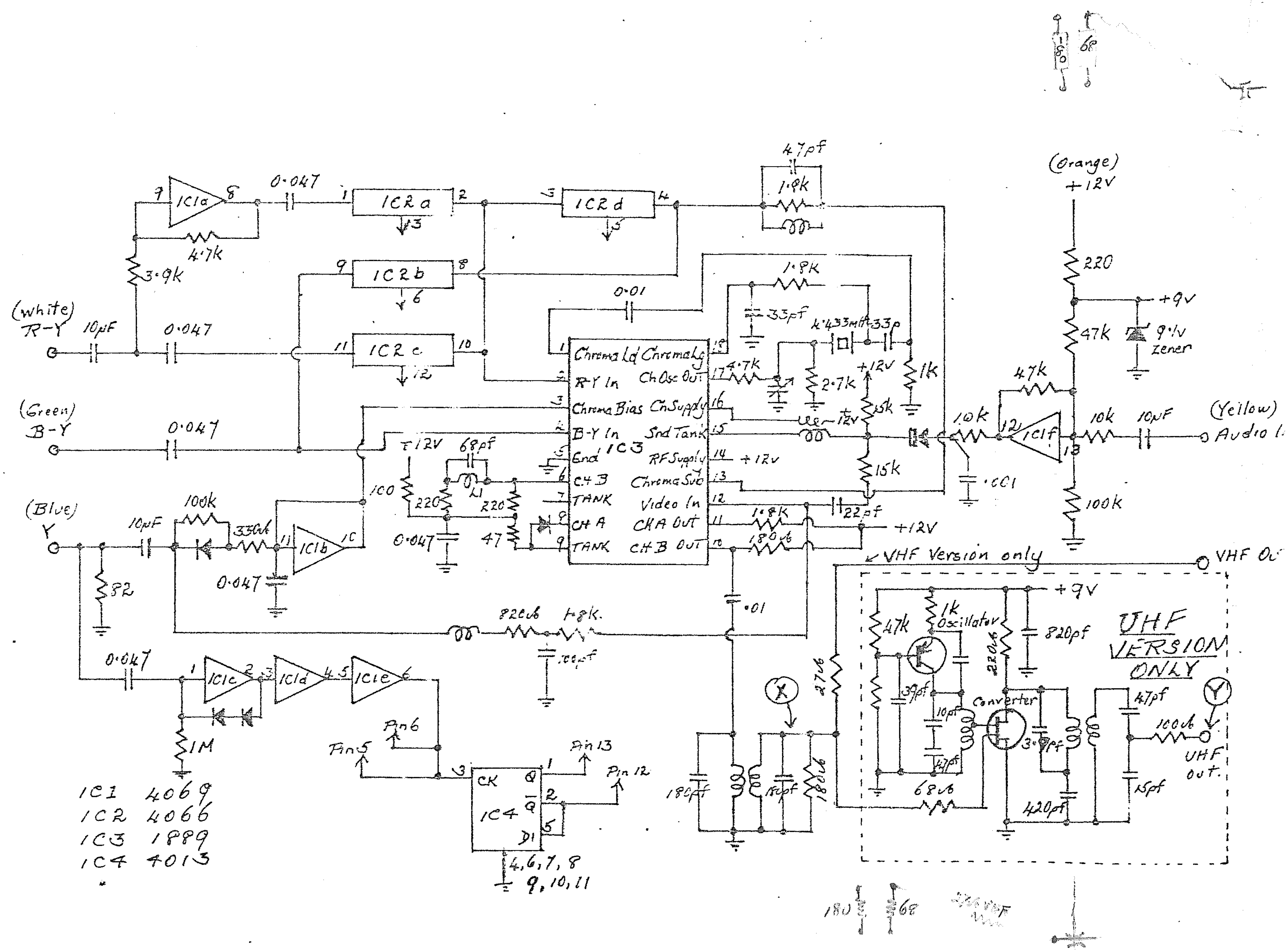
Modulator Plug. – Wiring



DISK DRIVE POWER SUPPLY

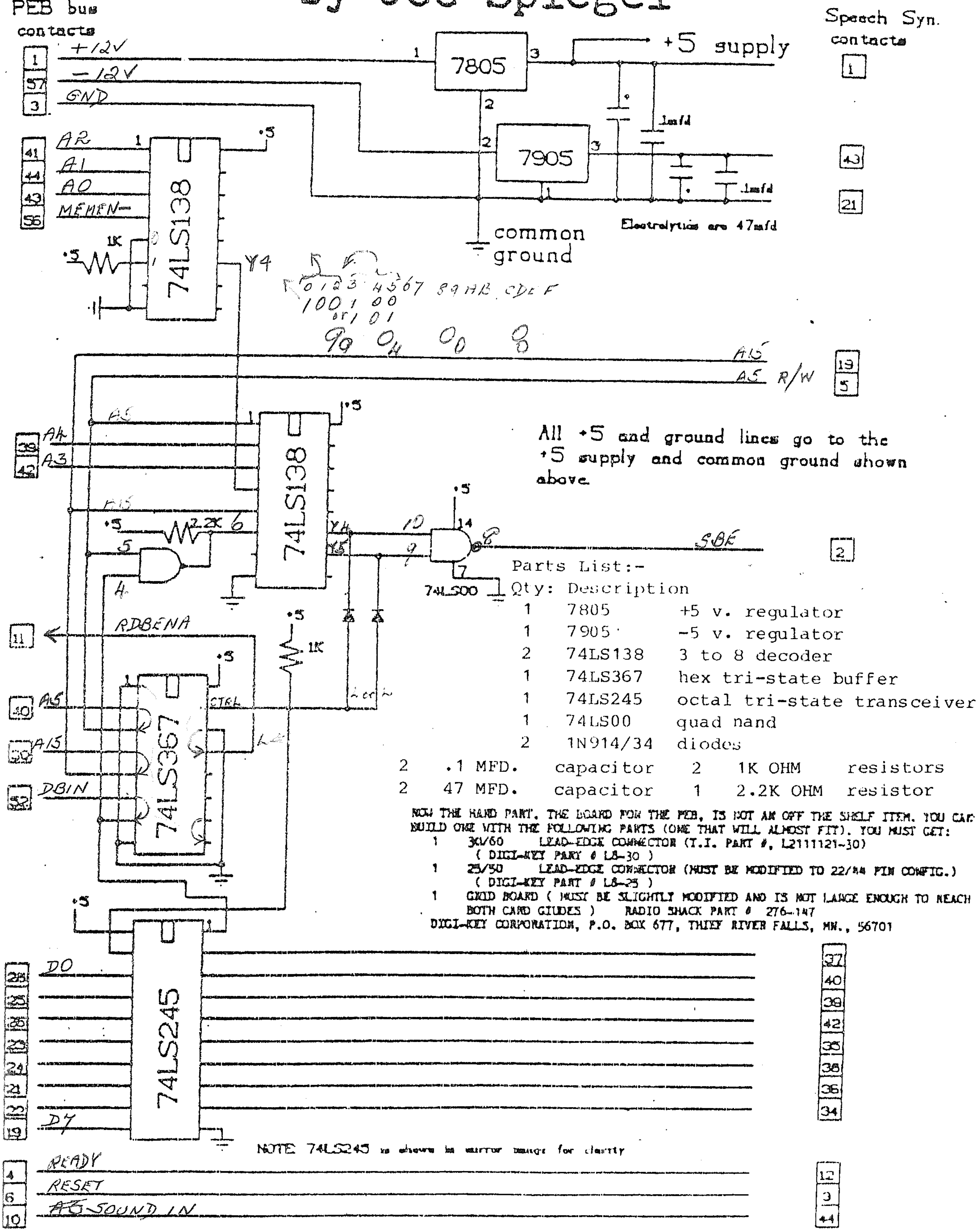



1
2
3
3o
4
4o
5
6
Modem
Phone


(white) R-Y
(Green) B-Y
(Blue) Y
(Orange) +12V
+9V
9.1V zener
(Yellow) Audio I/P
VHF Out
VHF Version only
UHF VERSION ONLY
UHF out.
Oscillator
Converter
Chroma Ld
Chroma Lg
R-Y In
Ch Osc Out
Chroma Bias
Ch Supply
B-Y In
Snd Tank
IC3
Gnd
RF Supply
CH B
Chroma Sub
TANK
Video In
CH A
CH A Out
CH B Out
IC1a
IC1b
IC1c
IC1d
IC1e
IC1f
IC2a
IC2b
IC2c
IC2d
IC4
CK
Q
D1
Pin 5
Pin 6
Pin 13
Pin 12
4.433MHz
IC1 4069
IC2 4066
IC3 1889
IC4 4013

```
     GROM PORT CONNECTIONS
 Rear View - Grom extender
          _________
         | .  .  . |
         |         |
         | .  .  . |
         | 2  1    |_______
GND.2 ___| .  .1-RESET-----|
-CRUCLK|   .  .3-D7--------|
CRUIN.6|   .  .5-D6-5------|
A15/CRU|   .  .7-D5--------|
A13..10|   .  .9-D4--------|
A12..12|   .  11D3-11------|
A11..14|   .  13D2---------|
A10..16|   .  15D1---------|
A9...18|   .  17D0-17------|
A8...20|   .  19+5V--------|
A7...22|   .  21-GSELECT---|
A6...24|   .  23A14-23-----|
A5...26|   .  25DBIN-------|
A4...28|   .  27GRCLK------|
A3...30|   .  29-5V-29-----|
-WE..32|   .  31GREADY-----|
-ROM/G.|   .  33VSS--------|
GND36 _|   .  35GND--------|
         36 35      _______|
         | .  .  . |
         |         |
         |_.  .  . |
           |_______|
```

PEB SPEECH INTERFACE
by Joe Spiegel



Parts List:-

Qty:	Description	
1	7805	+5 v. regulator
1	7905	-5 v. regulator
2	74LS138	3 to 8 decoder
1	74LS367	hex tri-state buffer
1	74LS245	octal tri-state transceiver
1	74LS00	quad nand
2	1N914/34	diodes

2 .1 MFD. capacitor 2 1K OHM resistors
2 47 MFD. capacitor 1 2.2K OHM resistor

NOW THE HARD PART. THE BOARD FOR THE PEB, IS NOT AN OFF THE SHELF ITEM. YOU CAN BUILD ONE WITH THE FOLLOWING PARTS (ONE THAT WILL ALMOST FIT). YOU MUST GET:

1 30/60 LEAD-EDGE CONNECTOR (T.I. PART #, L2111121-30)
(DIGI-KEY PART # L8-30)
1 25/50 LEAD-EDGE CONNECTOR (MUST BE MODIFIED TO 22/44 PIN CONFIG.)
(DIGI-KEY PART # L8-25)
1 GRID BOARD (MUST BE SLIGHTLY MODIFIED AND IS NOT LARGE ENOUGH TO REACH BOTH CARD GIUDES) RADIO SHACK PART # 276-147

DIGI-KEY CORPORATION, P.O. BOX 677, THIEF RIVER FALLS, MN., 56701

PRINTER AND CABLE CONNECTIONS

		PRINTER end.			TI end
PRINTER	DIR	36PIN	COLOUR	25PIN	16PIN
1 $\overline{\text{STROBE}}$	IN	1✓	BROWN	1	1✓ OUT
2 DATA 0	IN	2✓	RED	2	2✓
3 DATA 1	IN	3✓	ORANGE	3	3✓
4 DATA 2	IN	4✓	PINK	4	4✓
5 DATA 3	IN	5✓	YELLOW	5	5✓
6 DATA 4	IN	6✓	GREEN	6	6✓
7 DATA 5	IN	7✓	AQUA	7	7✓
8 DATA 6	IN	8✓	BLUE	8	8✓
9 DATA 7	IN	9✓	L BLUE	9	9✓
10 $\overline{\text{ACK}}$	OUT	10	PURPLE	10	
11 BUSY	OUT	11✓	GREY	11	10✓ IN
12 PAP OUT	OUT	12	WHITE	12	
13 SELECT	OUT	13	BLACK	13	
14 N/C		14	BN/WH	14	
15 N/5					
16 SIG GND					
17 CHAS "					
18 +5V DC					
***************		********************			*******
19 GND		19✓	GN/BK	19	11✓ 8✓ 16✓
20 GND		20	N/C		
21 GND		21	AQ/BK	20	
22 GND		22	N/C		
23 GND		23	BL/WH	21	
24 GND		24	N/C		
25 GND		25	L BL/WH	22	
26 GND		26	N/C		
27 GND		27	PU/WH	23	
28 GND		28	N/C		
29 GND		29	GY/BK	24	
30 GND		30	WH/BK	25	
31 $\overline{\text{RESET}}$	IN	31	OR/BK	16	
32 $\overline{\text{ERROR}}$	IN	32	RE/BK	15	
33 EXT GND		33	YE/BK	18	
34 N/C		34	N/C		
35 N/C		35	N/C		
36 $\overline{\text{SELC-IN}}$	IN	36	PK/BK	17	

Q&A

Over the past few months we have received some questions regarding the Power Up routine and its sequence of events.

The Power Up routine resides in console ROM and console GROM chip 0, with the majority of it in GROM. Listed below is the sequence of events, as we know it, that take place from the moment power is applied to the console.

1. When power is first applied to the 9900 microprocessor it executes a level 0 interrupt which is a reset. When this happens it knows to grab its workspace pointer from address >0000 and its program counter or instruction pointer from address >0002. In the 99/4A these addresses are burned into the console ROM. Once it has these addresses it begins to execute the code that is pointed to by address >0002.

2. The code pointed to by address >0002 loads R13 with >9800, the GROM read address, R14 with >0100, the status flag and R15 with >8C02, the VDP write address.

3. The balance of the Power Up routine is in GROM chip 0. First it clears out the sound list indicator at >83CE and then it turns off the Speech Synthesizer, if you have one, and turns off the sound generators.

4. Next it initializes the Data and Subroutine GPL stacks in Scratch Pad RAM.

5. Then it loads the VDP registers with default values stored in a GROM table.

6. Most of the Scratch Pad RAM is then cleared out by writing zeros to it.

7. The keyboard interrupts are then disabled and the cassette audio gate is turned on, this allows you to hear the cassette through your monitor speaker.

8. Next the VDP and external interrupts are enabled.

9. The cassette motors are then enabled, this sets up the remote jack so the motors can run.

10. Next it generates a BEEP sound by CALLing the TON1 routine in GROM chip 0.

11. And then it determines the size of VDP RAM, 4K or 16K, and sets bit 0 in VDP register 1 to 1 for 16K. I guess that TI thought they might produce a 4K console at one point in time.

12. The first 4K of VDP RAM is then cleared out and the default color and character tables are moved from GROM to VDP RAM.

13. Next the keyboards are initialized by scanning them. ie: CALL KEY(5.. ,CALL KEY(4.. , CALL KEY(3.. etc.

14. Then it moves the data for the Title Screen into the screen image table. At this point the screen can not be seen because it is turned off. Bit 1 in VDP register 1 is set to zero.

15. The ROMs(DSR) and GROMs are then searched for power up headers and if they have one they are executed.

16. After the search and execution of power up headers is complete the Title Screen is displayed by writing a 1 to bit 1 of VDP register 1. This is the first time that you are able to see the Tile Screen.

17. Next it initializes the Random Number Generator and then waits for you to 'PRESS ANY KEY'. After you press a key it generates another BEEP sound.

18. And then it searches through the cartridge ROM and GROM for application programs and builds a list of their names. ie: Editor/Assembler, Extended Basic, Basic etc. Note: some consoles, V2.0 (C) 1983, do not search ROM only GROM.

19. At this point the screen is once again turned off, VDP register 1, bit 1 is set to zero and then it sets up the menu screen with the application programs it found.

20. After the menu is set up it turns on the screen by writing a 1 to bit 1 of VDP register 1, and waits for you to make a selection.

21. If you make an illegal selection it generates a HONK sound, otherwise it sets up the starting address for the application program you selected and branches to it.

Q&A

Over the past few months we have received some questions regarding the Power Up routine and its sequence of events.

The Power Up routine resides in console ROM and console GROM chip 0, with the majority of it in GROM. Listed below is the sequence of events, as we know it, that take place from the moment power is applied to the console.

1. When power is first applied to the 9900 microprocessor it executes a level 0 interrupt which is a reset. When this happens it knows to grab its workspace pointer from address >0000 and its program counter or instruction pointer from address >0002. In the 99/4A these addresses are burned into the console ROM. Once it has these addresses it begins to execute the code that is pointed to by address >0002.

2. The code pointed to by address >0002 loads R13 with >9800, the GROM read address, R14 with >0100, the status flag and R15 with >8C02, the VDP write address.

3. The balance of the Power Up routine is in GROM chip 0. First it clears out the sound list indicator at >83CE and then it turns off the Speech Synthesizer, if you have one, and turns off the sound generators.

4. Next it initializes the Data and Subroutine GPL stacks in Scratch Pad RAM.

5. Then it loads the VDP registers with default values stored in a GROM table.

6. Most of the Scratch Pad RAM is then cleared out by writing zeros to it.

7. The keyboard interrupts are then disabled and the cassette audio gate is turned on, this allows you to hear the cassette through your monitor speaker.

8. Next the VDP and external interrupts are enabled.

9. The cassette motors are then enabled, this sets up the remote jack so the motors can run.

10. Next it generates a BEEP sound by CALLing the TON1 routine in GROM chip 0.

11. And then it determines the size of VDP RAM, 4K or 16K, and sets bit 0 in VDP register 1 to 1 for 16K. I guess that TI thought they might produce a 4K console at one point in time.

12. The first 4K of VDP RAM is then cleared out and the default color and character tables are moved from GROM to VDP RAM.

13. Next the keyboards are initialized by scanning them. ie: CALL KEY(5.. ,CALL KEY(4.. , CALL KEY(3.. etc.

14. Then it moves the data for the Title Screen into the screen image table. At this point the screen can not be seen because it is turned off. Bit 1 in VDP register 1 is set to zero.

15. The ROMs(DSR) and GROMs are then searched for power up headers and if they have one they are executed.

16. After the search and execution of power up headers is complete the Title Screen is displayed by writing a 1 to bit 1 of VDP register 1. This is the first time that you are able to see the Tile Screen.

17. Next it initializes the Random Number Generator and then waits for you to 'PRESS ANY KEY'. After you press a key it generates another BEEP sound.

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